



# Low-Power, +2.5V to +5.5V, 8-Bit Voltage-Output DAC in $\mu$ MAX

MAX550B

## General Description

The MAX550B serial, 8-bit, voltage-output, digital-to-analog converter (DAC) operates on a single +2.5V to +5.5V supply. Its  $\pm 1$ LSB TUE specification is guaranteed over temperature. Operating current (supply current plus reference current) is typically 75 $\mu$ A with  $V_{DD} = 2.5$ V and less than 1 $\mu$ A in shutdown mode. The reference input is disconnected from the REF pin during shutdown.

The serial interface operates at clock rates up to 10MHz and is compatible with 3-wire SPI™, QSPI™, and Microwire™ interface standards.

The MAX550B's ultra-low power consumption and small  $\mu$ MAX package make it ideal for portable and battery-powered applications.

## Features

- ♦ **+2.5V to +5.5V Single-Supply Operation**
- ♦  **$\pm 1$ LSB (max) TUE**
- ♦ **Low 75 $\mu$ A Operating Current ( $V_{DD} = +2.5$ V)**
- ♦ **1 $\mu$ A Shutdown Mode**
- ♦  **$\mu$ MAX Package—50% Smaller than 8-Pin SO**
- ♦ **10MHz, 3-Wire Serial Interface**
- ♦ **Internal Power-On Reset Clears All Registers to Zero**

## Applications

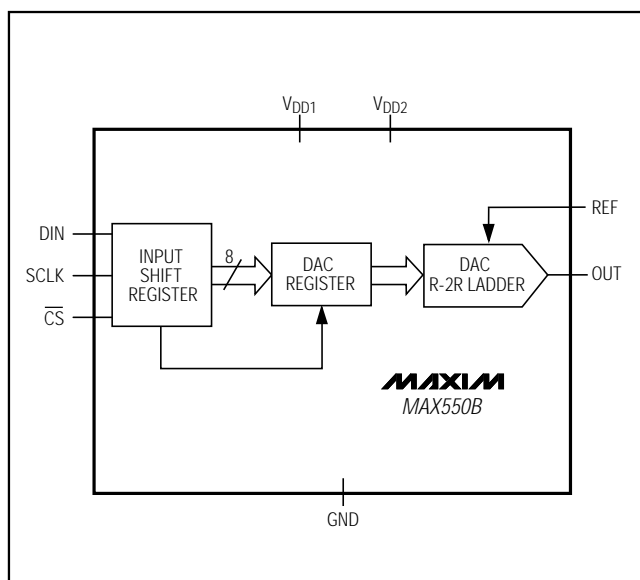
VCXO Control  
Comparator Level Settings  
GaAs Amp Bias Control  
Digital Gain and Offset Control

## Ordering Information

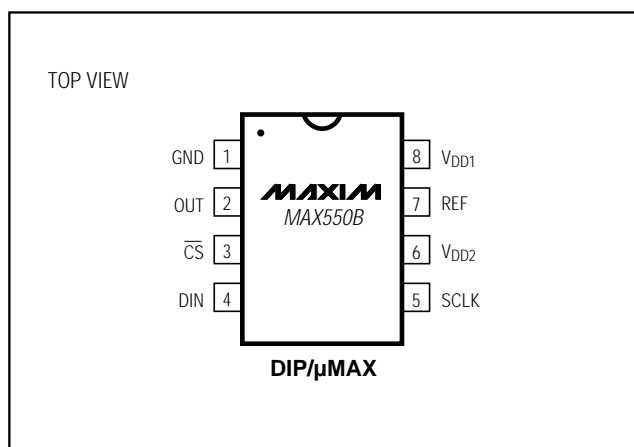
| PART       | TEMP. RANGE    | PIN-PACKAGE   |
|------------|----------------|---------------|
| MAX550BCPA | 0°C to +70°C   | 8 Plastic DIP |
| MAX550BCUA | 0°C to +70°C   | 8 $\mu$ MAX   |
| MAX550BC/D | 0°C to +70°C   | Dice*         |
| MAX550BEPA | -40°C to +85°C | 8 Plastic DIP |
| MAX550BEUA | -40°C to +85°C | 8 $\mu$ MAX   |

\*Dice are specified at  $T_A = +25^\circ\text{C}$ , DC parameters only.

## Functional Diagram



## Pin Configuration



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# Low-Power, +2.5V to +5.5V, 8-Bit Voltage-Output DAC in $\mu$ MAX

## ABSOLUTE MAXIMUM RATINGS

$V_{DD1}$ ,  $V_{DD2}$ , SCLK, DIN,  $\overline{CS}$ , OUT to GND ..... -0.3V to +6V  
 REF ..... -0.3V to ( $V_{DD\_}$  + 0.3V)  
 Maximum Current (any pin) ..... 50mA  
 Continuous Power Dissipation ( $T_A$  = +70°C)  
   Plastic DIP (derate 9.1mW/°C above +70°C) ..... 727mW  
    $\mu$ MAX (derate 4.1mW/°C above +70°C) ..... 330mW

### Operating Temperature Ranges

MAX550BBC\_A ..... 0°C to +70°C  
 MAX550BBE\_A ..... -40°C to +85°C  
 Storage Temperature Range ..... -65°C to +150°C  
 Lead Temperature (soldering, 10sec) ..... +300°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

## ELECTRICAL CHARACTERISTICS

( $V_{DD1}$  =  $V_{DD2}$  = +2.5V to +5.5V,  $T_A$  =  $T_{MIN}$  to  $T_{MAX}$ , unless otherwise noted. Typical values are at  $T_A$  = +25°C.)

| PARAMETER                                     | SYMBOL           | CONDITIONS                               |  | MIN                 | TYP | MAX              | UNITS |
|---|------------------|--|--|---------------------|-----|------------------|-------|
| STATIC PERFORMANCE                            |                  |  |  |                     |     |                  |       |
| Resolution                                    | N                |  |  | 8                   |     |                  | Bits  |
| Differential Nonlinearity                     | DNL              | Guaranteed monotonic                     | MAX550BBC_A/MAX550BBE                      | ±0.9                |     | LSB              |       |
|   |                  |  | MAX550BBEUA (Note 1)                       | ±0.9                |     |                  |       |
| Total Unadjusted Error                        | TUE              |  | MAX550BBC_A/MAX550BBE                      | ±1                  |     | LSB              |       |
|   |                  |  | MAX550BBEUA (Note 1)                       | ±1                  |     |                  |       |
| Zero-Code Error                               | ZCE              | T <sub>A</sub> = +25°C                   |  | ±1                  |     | LSB              |       |
| Full-Scale Error                              | FSE              |  |  | ±1                  |     | LSB              |       |
| REFERENCE INPUT                               |                  |  |  |                     |     |                  |       |
| Reference Input Voltage                       | V <sub>REF</sub> | For specified performance                |  | 2.5                 |     | V <sub>DD</sub>  | V     |
| Reference Input Resistance (Note 2)           | R <sub>REF</sub> | DAC code = 55 hex                        |  | 32                  |     |                  | kΩ    |
| Reference Input Current (Note 3)              | I <sub>REF</sub> | DAC code = 55 hex                        | V <sub>DD_</sub> = V <sub>REF</sub> = 5.5V | 160                 | 275 | μA               |       |
|   |                  |  | V <sub>DD_</sub> = V <sub>REF</sub> = 2.5V | 75                  | 125 |                  |       |
| DAC OUTPUT (OUT)                              |                  |  |  |                     |     |                  |       |
| DAC Output Voltage Swing                      |                  |  |  | 0                   |     | V <sub>REF</sub> | V     |
| DAC Output Resistance                         | R <sub>OUT</sub> |  |  | 32                  |     |                  | kΩ    |
| DIGITAL INPUTS ( $\overline{CS}$ , SCLK, DIN) |                  |  |  |                     |     |                  |       |
| Input High Voltage                            | V <sub>IH</sub>  |  |  | 0.7V <sub>DD_</sub> |     |                  | V     |
| Input Low Voltage                             | V <sub>IL</sub>  |  |  | 0.3V <sub>DD_</sub> |     |                  | V     |
| Input Current                                 | I <sub>IN</sub>  | V <sub>IN</sub> = 0V or V <sub>DD_</sub> |  | ±1                  |     |                  | μA    |
| Input Capacitance (Note 4)                    | C <sub>IN</sub>  |  |  | 10                  |     |                  | pF    |

# Low-Power, +2.5V to +5.5V, 8-Bit Voltage-Output DAC in $\mu$ MAX

## ELECTRICAL CHARACTERISTICS (continued)

( $V_{DD1} = V_{DD2} = +2.5V$  to  $+5.5V$ ,  $T_A = T_{MIN}$  to  $T_{MAX}$ , unless otherwise noted. Typical values are at  $T_A = +25^\circ C$ .)

| PARAMETER                         | SYMBOL              | CONDITIONS   | MIN | TYP | MAX | UNITS            |
|-----------------------------------|---------------------|--|-----|-----|-----|------------------|
| <b>DYNAMIC PERFORMANCE</b>        |                     |  |     |     |     |                  |
| Digital Feedthrough and Crosstalk |                     | $\overline{CS} = \text{high}$ , all digital inputs from 0V to $V_{DD\_}$ |     | 50  |     | nV-sec           |
| Voltage-Output Settling Time      |                     | To $\pm 1/2\text{LSB}$ , $C_L = 20\text{pF}$                             |     | 4   |     | $\mu\text{s}$    |
| Voltage-Output Slew Rate          | SR                  | $C_L = 20\text{pF}$  |     | 1.4 |     | V/ $\mu\text{s}$ |
|                                   |                     | $V_{DD\_} = 5.5V$  |     | 3.1 |     |                  |
| Wake-Up Time                      |                     | $C_{LOAD} = 20\text{pF}$   |     | 4   |     | $\mu\text{s}$    |
| <b>POWER SUPPLIES</b>             |                     |  |     |     |     |                  |
| Supply Voltage Range              | $V_{DD\_}$          | Output unloaded, all inputs = GND or $V_{DD}$                            | 2.5 |     | 5.5 | V                |
| Supply Current                    | $I_{DD1} + I_{DD2}$ | $V_{DD\_} = 5.5V$ , output unloaded, all inputs = GND or $V_{DD\_}$      |     | 0.3 | 10  | $\mu\text{A}$    |
| Shutdown Current                  |                     | Shutdown mode  |     | 0.3 |     | $\mu\text{A}$    |

**Note 1:**  $0^\circ C$  to  $-40^\circ C$  testing guaranteed by design using six sigma design limits.

**Note 2:** Worst-case input resistance at REF occurs at DAC code 55 hex.

**Note 3:** Worst-case reference input current occurs at DAC code 55 hex.

**Note 4:** Guaranteed by design. Not production tested.

## TIMING CHARACTERISTICS (Note 5)

( $V_{DD1} = V_{DD2} = +2.5V$  to  $+5.5V$ ,  $T_A = T_{MIN}$  to  $T_{MAX}$ , unless otherwise noted. Digital inputs switching from 0V to  $V_{DD\_}$ .)

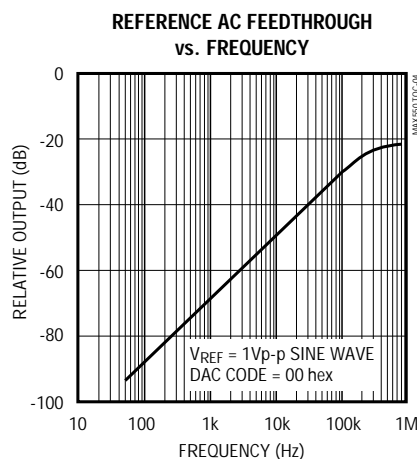
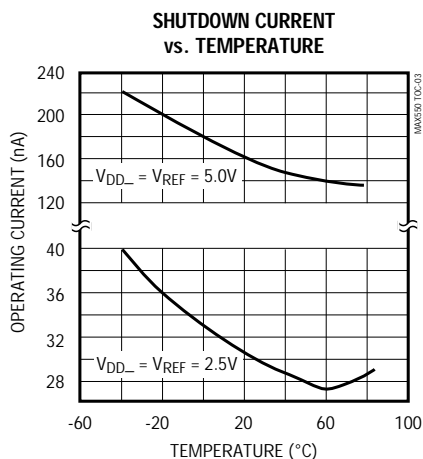
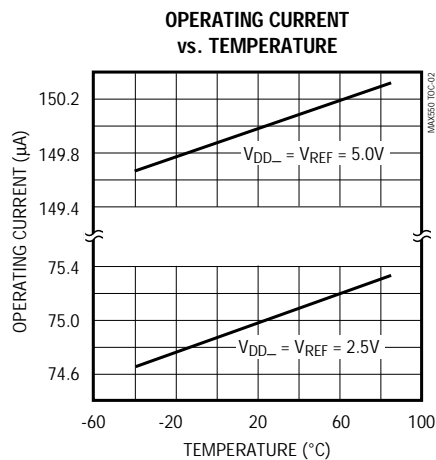
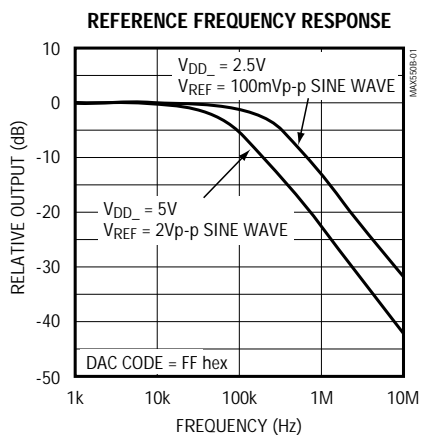
| PARAMETER                                | SYMBOL     | CONDITIONS           | MIN | TYP | MAX | UNITS         |
|--|------------|----------------------|-----|-----|-----|---------------|
| SCLK Pulse Width High                    | $t_{CH}$   |                      | 40  |     |     | ns            |
| SCLK Pulse Width Low                     | $t_{CL}$   |                      | 40  |     |     | ns            |
| DIN to SCLK High Setup                   | $t_{DS}$   |                      | 30  |     |     | ns            |
| DIN to SCLK High Hold                    | $t_{DH}$   | $V_{DD\_} = 2.5V$    | 0   |     |     | ns            |
|  |            | $V_{DD\_} = 5.5V$    | 10  |     |     |               |
| $\overline{CS}$ Low to SCLK High Setup   | $t_{CSS0}$ |                      | 30  |     |     | ns            |
| $\overline{CS}$ High to SCLK High Setup  | $t_{CSS1}$ |                      | 30  |     |     | ns            |
| SCLK High to $\overline{CS}$ Low Hold    | $t_{CSH0}$ |                      | 20  |     |     | ns            |
| Delay, SCLK High to $\overline{CS}$ High | $t_{CSH1}$ | $V_{DD\_} = 2.5V$    | 10  |     |     | ns            |
|  |            | $V_{DD\_} = 5.5V$    | 20  |     |     |               |
| $\overline{CS}$ Pulse Width High         | $t_{CSW}$  |                      | 40  |     |     | ns            |
| SCLK Period                              | $t_{CP}$   |                      | 80  |     |     | ns            |
| $V_{DD\_}$ High to $\overline{CS}$ Low   |            | Power-on reset delay |     | 5   |     | $\mu\text{s}$ |

**Note 5:** Guaranteed by design. Not production tested.

# Low-Power, +2.5V to +5.5V, 8-Bit Voltage-Output DAC in $\mu$ MAX

## Typical Operating Characteristics

( $V_{DD1} = V_{DD2} = 2.5V$ ,  $V_{REF} = V_{DD-}$ ,  $R_L = 1M\Omega$ ,  $C_L = 15pF$ ,  $T_A = +25^\circ C$ , unless otherwise noted.)



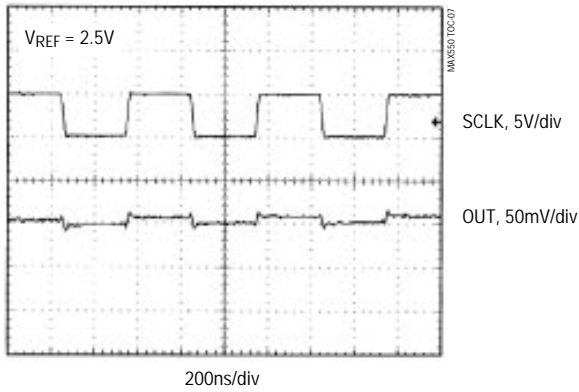
# Low-Power, +2.5V to +5.5V, 8-Bit Voltage-Output DAC in $\mu$ MAX

MAX550B

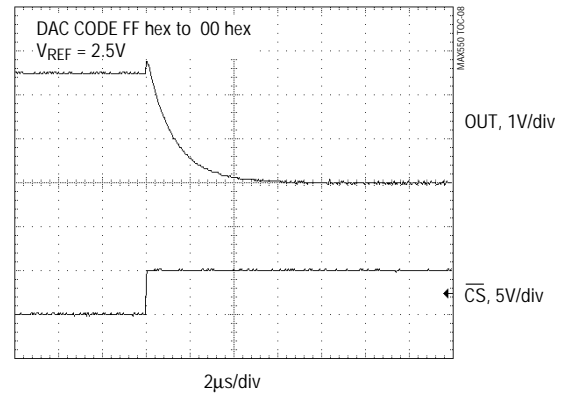
## Typical Operating Characteristics (continued)

( $V_{DD1} = V_{DD2} = 2.5V$ ,  $V_{REF} = V_{DD-}$ ,  $R_L = 1M\Omega$ ,  $C_L = 15pF$ ,  $T_A = +25^\circ C$ , unless otherwise noted.)

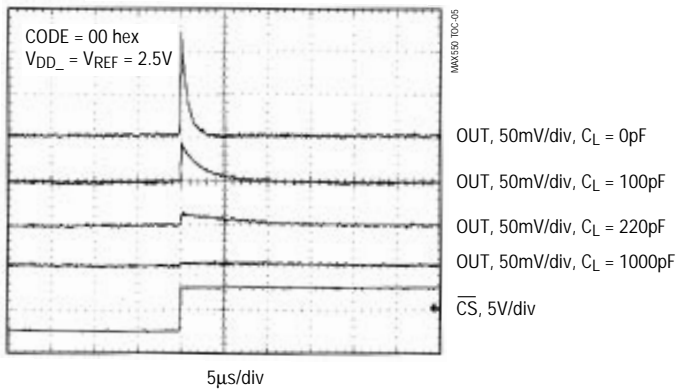
**DIGITAL FEEDTHROUGH**



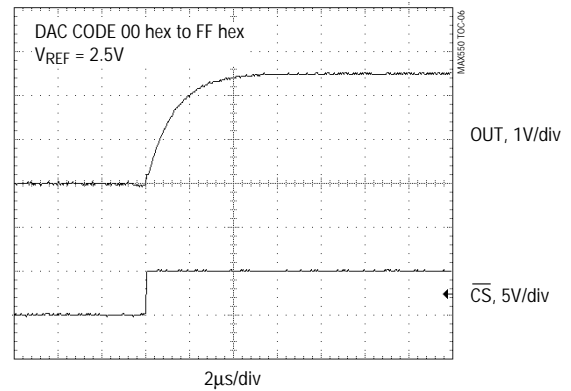
**NEGATIVE SETTLING TIME**



**OUTPUT GLITCH FILTERING**



**POSITIVE SETTLING TIME**



# Low-Power, +2.5V to +5.5V, 8-Bit Voltage-Output DAC in $\mu$ MAX

## Pin Description

| PIN | NAME             | FUNCTION  |
|-----|------------------|---|
| 1   | GND              | Ground  |
| 2   | OUT              | DAC Output Voltage  |
| 3   | $\overline{CS}$  | Chip-Select Input. A logic low on $\overline{CS}$ enables serial data to be clocked into the input shift register. Programming commands are executed at $\overline{CS}$ 's rising edge. |
| 4   | DIN              | Serial Data Input. Data is clocked into the 16-bit input shift register on SCLK's rising edge.  |
| 5   | SCLK             | Serial Clock Input. Data is clocked in on SCLK's rising edge.   |
| 6   | V <sub>DD2</sub> | Connect to V <sub>DD1</sub>   |
| 7   | REF              | External Reference Voltage Input for DAC (2.5V to V <sub>DD1</sub> )  |
| 8   | V <sub>DD1</sub> | Positive Power Supply (+2.5V to +5.5V)  |

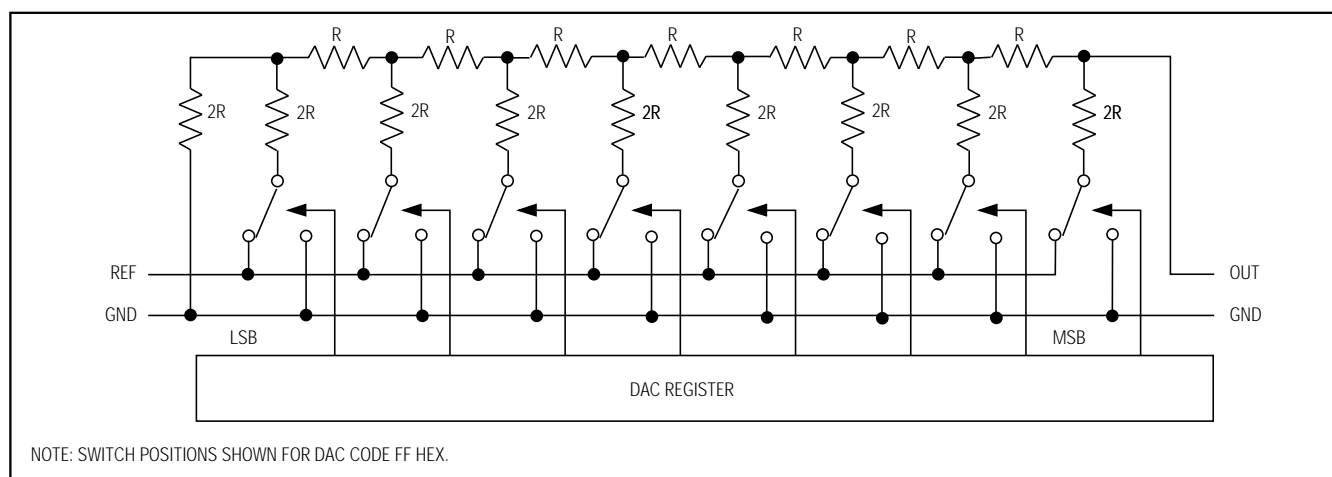


Figure 1. DAC Simplified Circuit Diagram

## Detailed Description

### Analog Section

The MAX550B is an 8-bit, voltage-output digital-to-analog converter (DAC). The DAC consists of an R-2R ladder network that converts 8-bit digital inputs into equivalent analog output voltages in proportion to the applied reference voltage (Figure 1). The MAX550B's output is unbuffered and has a typical output resistance of 32k $\Omega$ . The power-supply range is from +2.5V to +5.5V.

### Reference Input

The voltage applied at REF sets the full-scale output for the DAC and may range from 2.5V to V<sub>DD1</sub>. The REF input resistance is code-dependent, with the lowest value (typically 32k $\Omega$ ) occurring when the DAC register is loaded with a code of 01010101 (55 hex). To minimize INL errors, the reference voltage source should have less than 6 $\Omega$  output impedance.

# Low-Power, +2.5V to +5.5V, 8-Bit Voltage-Output DAC in $\mu$ MAX

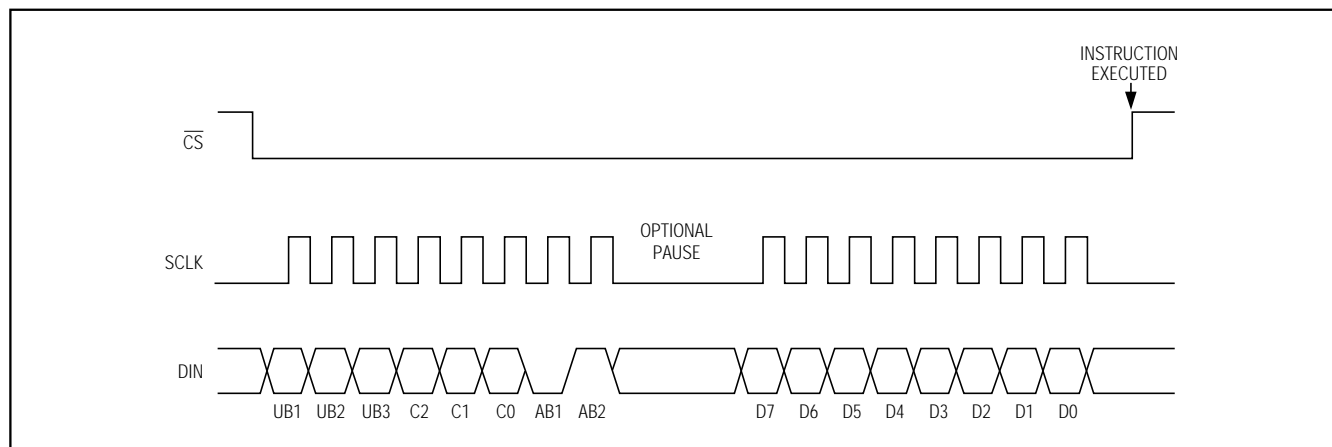


Figure 2. Serial-Interface Timing Diagram

## DAC Output

The MAX550B's output is unbuffered; it connects directly to the R-2R ladder. This configuration minimizes power consumption and reduces offset errors. For highest accuracy, apply high resistive loads ( $1\text{M}\Omega$  and up). Lower resistive loads can be driven, but output loading increases full-scale error. The magnitude of the expected error is the ratio of the DAC output resistance to the DC load resistance at the output.

Typically, an energy pulse is coupled into the DAC output on the rising edge of  $\overline{\text{CS}}$ . Since the MAX550B's output is unbuffered (connected directly to the R-2R ladder), connecting a small capacitor (200pF to 1000pF) from the output to ground creates a lowpass filter that effectively suppresses the pulse for sensitive applications (see Output Glitch Filtering graph in the *Typical Operating Characteristics*).

## Shutdown Mode

When the MAX550B is in shutdown mode, REF becomes high impedance. The supply current is unchanged, but the REF input current decreases to less than  $1\mu\text{A}$ . This allows the system reference to remain active with minimal power consumption.

When exiting shutdown mode, the output recovery time is equivalent to the DAC settling time.

## Serial Interface

The MAX550B interface is compatible with 3-wire SPI™, QSPI™, and Microwire™ microprocessor ( $\mu\text{P}$ ) interface standards. An active-low chip select ( $\overline{\text{CS}}$ ) enables the input shift register to receive data from the serial input, DIN (Figure 2). Data is clocked into the input shift register

on rising edges of the serial clock signal (SCLK). The clock frequency can be as high as 10MHz.

When writing to the DAC, transmit data MSB first in one 16-bit word or two 8-bit bytes. The write cycle can be segmented when  $\overline{\text{CS}}$  is kept active (low) to allow two 8-bit-wide transfers. After clocking all 16 bits into the input shift register, a rising edge on  $\overline{\text{CS}}$  programs the DAC. The DAC output reflects the data stored in the DAC register. Figure 3 gives detailed timing information.

## Initialization

The MAX550B has an internal power-on reset. At power-up, all internal registers are reset to zero; therefore, an initialization write is not necessary.

## Serial Input Data Format and Control Codes

The control byte programs the DAC (Table 1). Table 2 lists the MAX550B's serial-input command format. The 16-bit input word consists of an 8-bit control byte and an 8-bit data byte. The 8-bit control byte is not decoded internally; every control bit performs one function. Data is clocked in starting with unassigned bit 1 (UB1), followed by the remaining control bits and the DAC data byte. The LSB (D0) of the data byte is the last bit clocked into the input shift register (Figure 2).

Table 3 is an example of a 16-bit word. It performs the following functions:

- 1) Load 80 hex (128 decimal) into the DAC register.
- 2) Update the DAC output on  $\overline{\text{CS}}$ 's rising edge.

Table 4 shows how to calculate the output voltage based on the input code.

# Low-Power, +2.5V to +5.5V, 8-Bit Voltage-Output DAC in $\mu$ MAX

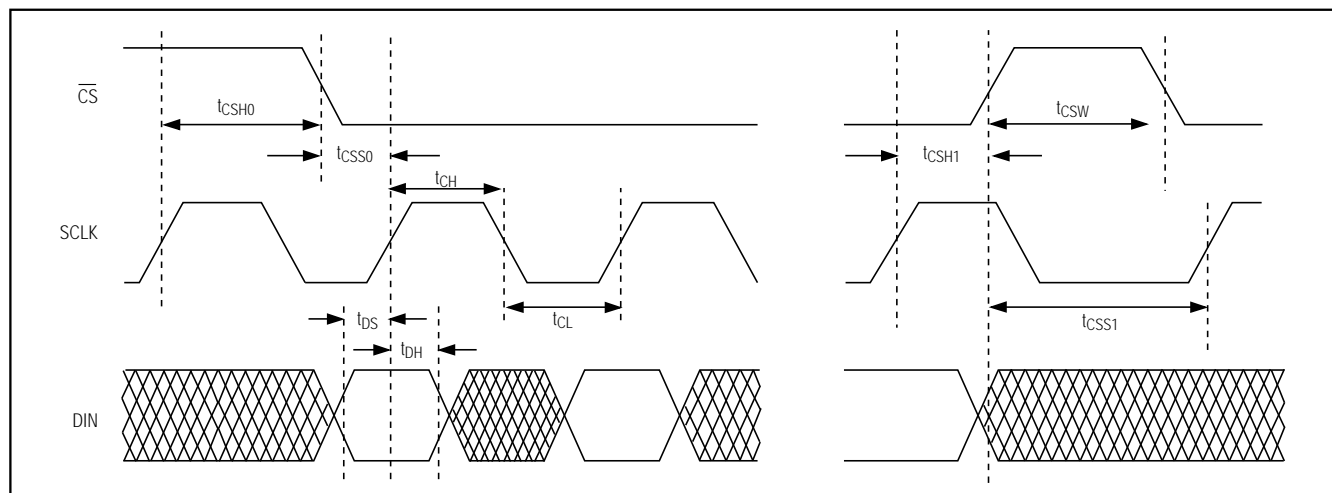


Figure 3. Detailed Serial-Interface Timing Diagram

**Table 1. Control-Byte/Input-Word Bit Definitions**

|              |      |   |  |
|--------------|------|---|--|
| Control Byte | UB1* | X | Unassigned Bit 1                                     |
|              | UB2  | X | Unassigned Bit 2                                     |
|              | UB3  | X | Unassigned Bit 3                                     |
|              | C2   | 0 | Power-Up Mode  |
|              | C2   | 1 | Power-Down Mode                                      |
|              | C1   | 0 | DAC Register Load Operation Disabled                 |
|              | C1   | 1 | DAC Register Load Operation Enabled                  |
|              | C0   | 0 | DAC Output Updated on Rising Edge of $\overline{CS}$ |
|              | C0   | 1 | Unassigned Operation                                 |
|              | AB1  | 0 | Assigned Bit 1                                       |
| Data Byte    | AB2  | 1 | Assigned Bit 2                                       |
|              | D7   | X | DAC Data Bit 7 (MSB)                                 |
|              | D6   | X | DAC Data Bit 6                                       |
|              | D5   | X | DAC Data Bit 5                                       |
|              | D4   | X | DAC Data Bit 4                                       |
|              | D3   | X | DAC Data Bit 3                                       |
|              | D2   | X | DAC Data Bit 2                                       |
|              | D1   | X | DAC Data Bit 1                                       |
|              | D0** | X | DAC Data Bit 0 (LSB)                                 |

X = Don't care

\*Clocked in first

\*\*Clocked in last

## Microprocessor Interfacing

The MAX550B serial interface is compatible with Microwire, SPI, and QSPI interface standards. For SPI, clear the CPOL and CPHA bits (CPOL = 0 and CPHA = 0). CPOL = 0 sets the idle clock state to zero and CPHA = 0 changes data at SCLK's falling edge. This setting allows SPI to run at full clock speeds (1.5MHz). If a serial port is not available on your  $\mu$ P, three bits of a parallel port can be used to emulate a serial port by bit manipulation. Minimize digital feedthrough at the DAC output by operating the serial clock only when necessary.

## Applications Information

### Power-Supply and Ground Considerations

Connect GND to the highest-quality ground available. Bypass  $V_{DD}$  with a 0.1 $\mu$ F to 0.22 $\mu$ F capacitor to GND. The reference input can be used without bypassing. However, for optimum line/load-transient response and noise performance, bypass the reference input with a 0.1 $\mu$ F to 4.7 $\mu$ F capacitor to GND.

Careful PC board layout minimizes crosstalk between the DAC output, the reference, and the digital inputs. Separate analog traces by running ground traces between them. Make sure high-frequency digital lines are not routed parallel to analog lines.



# Low-Power, +2.5V to +5.5V, 8-Bit Voltage-Output DAC in $\mu$ MAX

**Table 2. Serial-Interface Programming Commands**

| CONTROL BYTE |     |     |    |    |    |     |     | DATA BYTE      |    |    |    |    |    |    |    | COMMAND  |
|--------------|-----|-----|----|----|----|-----|-----|----------------|----|----|----|----|----|----|----|--|
| Loaded First |     |     |    |    |    |     |     | Loaded Last    |    |    |    |    |    |    |    |  |
| UB1          | UB2 | UB3 | C2 | C1 | C0 | AB1 | AB2 | D7             | D6 | D5 | D4 | D3 | D2 | D1 | D0 |  |
| X            | X   | X   | 0  | 0  | 0  | 0   | 1   | X              | X  | X  | X  | X  | X  | X  | X  | On $\overline{CS}$ 's rising edge, wake up DAC.<br>DAC register unchanged.                             |
| X            | X   | X   | X  | X  | 1  | X   | X   | X              | X  | X  | X  | X  | X  | X  | X  | Unassigned command   |
| X            | X   | X   | 0  | 1  | 0  | 0   | 1   | 8-bit DAC data |    |    |    |    |    |    |    | On $\overline{CS}$ 's rising edge, load DAC register.<br>Wake up DAC (if previously powered down).     |
| X            | X   | X   | 1  | 0  | 0  | 0   | 1   | X              | X  | X  | X  | X  | X  | X  | X  | On $\overline{CS}$ 's rising edge, power down DAC.<br>DAC output goes to zero. DAC register unchanged. |
| X            | X   | X   | 1  | 1  | 0  | 0   | 1   | 8-bit DAC data |    |    |    |    |    |    |    | On $\overline{CS}$ 's rising edge, power down DAC and update DAC register. DAC output goes to zero.    |

X = Don't Care

**Table 3. Example Input Word**

| Loaded First |     |     |    |    |    |     |     | Loaded Last |    |    |    |    |    |    |    |
|--------------|-----|-----|----|----|----|-----|-----|-------------|----|----|----|----|----|----|----|
| UB1          | UB2 | UB3 | C2 | C1 | C0 | AB1 | AB2 | D7          | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| X            | X   | X   | 0  | 1  | 0  | 0   | 1   | 1           | 0  | 0  | 0  | 0  | 0  | 0  | 0  |

X = Don't Care

**Table 4. Analog Output vs. Code**

| DAC REGISTER CONTENTS |    |    |    |    |    |    |    | ANALOG OUTPUT (V)                        |
|-----------------------|----|----|----|----|----|----|----|--|
| D7                    | D6 | D5 | D4 | D3 | D2 | D1 | D0 |  |
| 1                     | 1  | 1  | 1  | 1  | 1  | 1  | 1  | $+V_{REF} \times (255/256)$              |
| 1                     | 0  | 0  | 0  | 0  | 0  | 0  | 1  | $+V_{REF} \times (129/256)$              |
| 1                     | 0  | 0  | 0  | 0  | 0  | 0  | 0  | $+V_{REF} \times (128/256) = +V_{REF}/2$ |
| 0                     | 1  | 1  | 1  | 1  | 1  | 1  | 1  | $+V_{REF} \times (127/256)$              |
| 0                     | 0  | 0  | 0  | 0  | 0  | 0  | 1  | $+V_{REF} \times (1/256)$                |
| 0                     | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |

**Note:**  $1\text{LSB} = V_{REF} \times 2^{-8} = V_{REF}(1/256)$ 

 ANALOG OUTPUT =  $+V_{REF}(I/256)$ , where I = Integer Value of Digital Input and wake up DAC (if previously powered down)

# Low-Power, +2.5V to +5.5V, 8-Bit Voltage-Output DAC in $\mu$ MAX

## AC Considerations

### Digital Feedthrough

High-speed data at any of the digital input pins may couple through the DAC's internal stray capacitance and cause noise (digital feedthrough) at the DAC output, even though  $\overline{CS}$  is held high. This digital feedthrough is tested by holding  $\overline{CS}$  high and toggling the digital inputs from all 1s to all 0s.

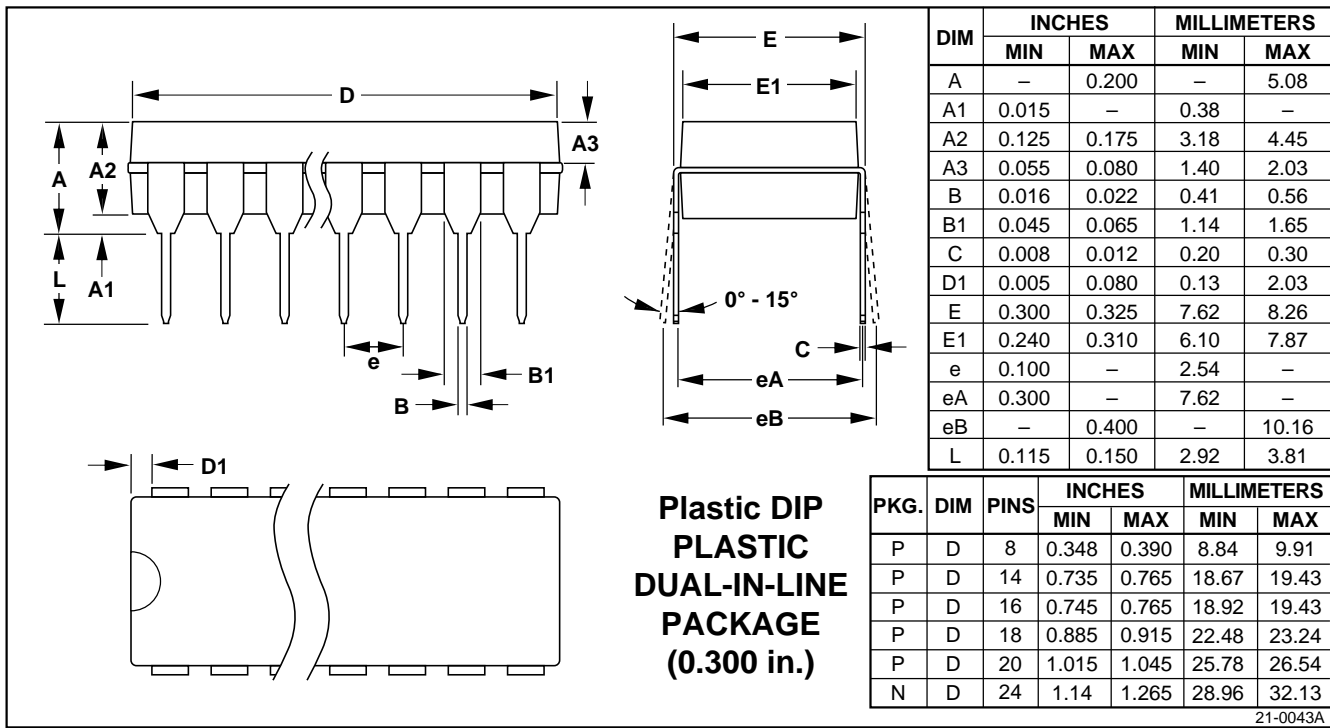
### Analog Feedthrough

Due to internal stray capacitance, higher-frequency analog input signals at REF may couple to the output, even when the input digital code is all 0s. Test analog feedthrough by setting the DAC output to 0V and sweeping REF.

## Chip Information

TRANSISTOR COUNT: 1562

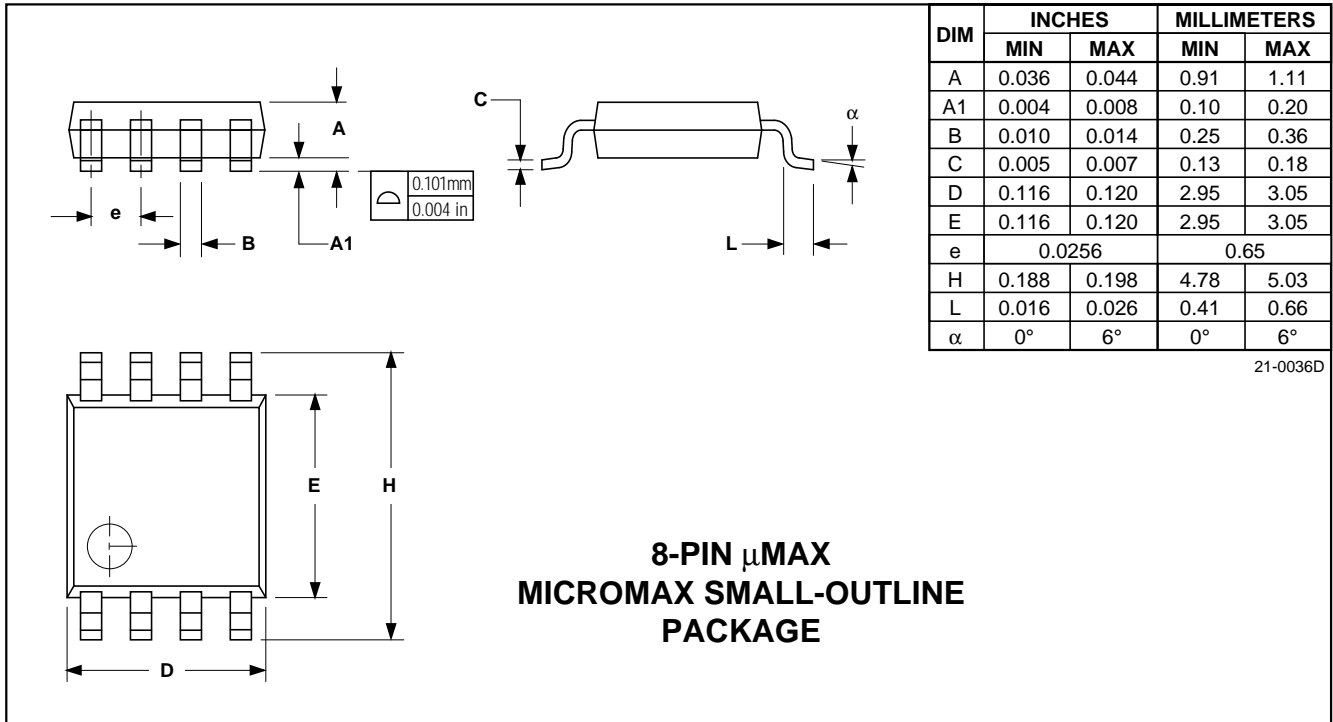
## Package Information



# Low-Power, +2.5V to +5.5V, 8-Bit Voltage-Output DAC in $\mu$ MAX

Package Information (continued)

MAX550B



# Low-Power, +2.5V to +5.5V, 8-Bit Voltage-Output DAC in $\mu$ MAX

## NOTES

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