

## PRELIMINARY TECHNICAL DATA

## AD7841

### FEATURES

**Eight 14-Bit DACs in One Package**  
**Voltage Outputs**  
**Offset Adjust for Each DAC Pair**  
**Reference Range of  $\pm 5$  V**  
**Maximum Output Voltage Range of  $\pm 10$  V**  
**Clear Function to User-Defined Voltage**  
 **$\pm 10.8$  V to  $\pm 16.5$  V Operation**  
**44-Pin PQFP Package**

### APPLICATIONS

**Automatic Test Equipment**  
**Process Control**  
**General Purpose Instrumentation**

### GENERAL DESCRIPTION

The AD7841 contains eight 14-bit DACs on one monolithic chip. It has output voltages with a full-scale range of  $\pm 10$  V from reference voltages of  $\pm 5$  V.

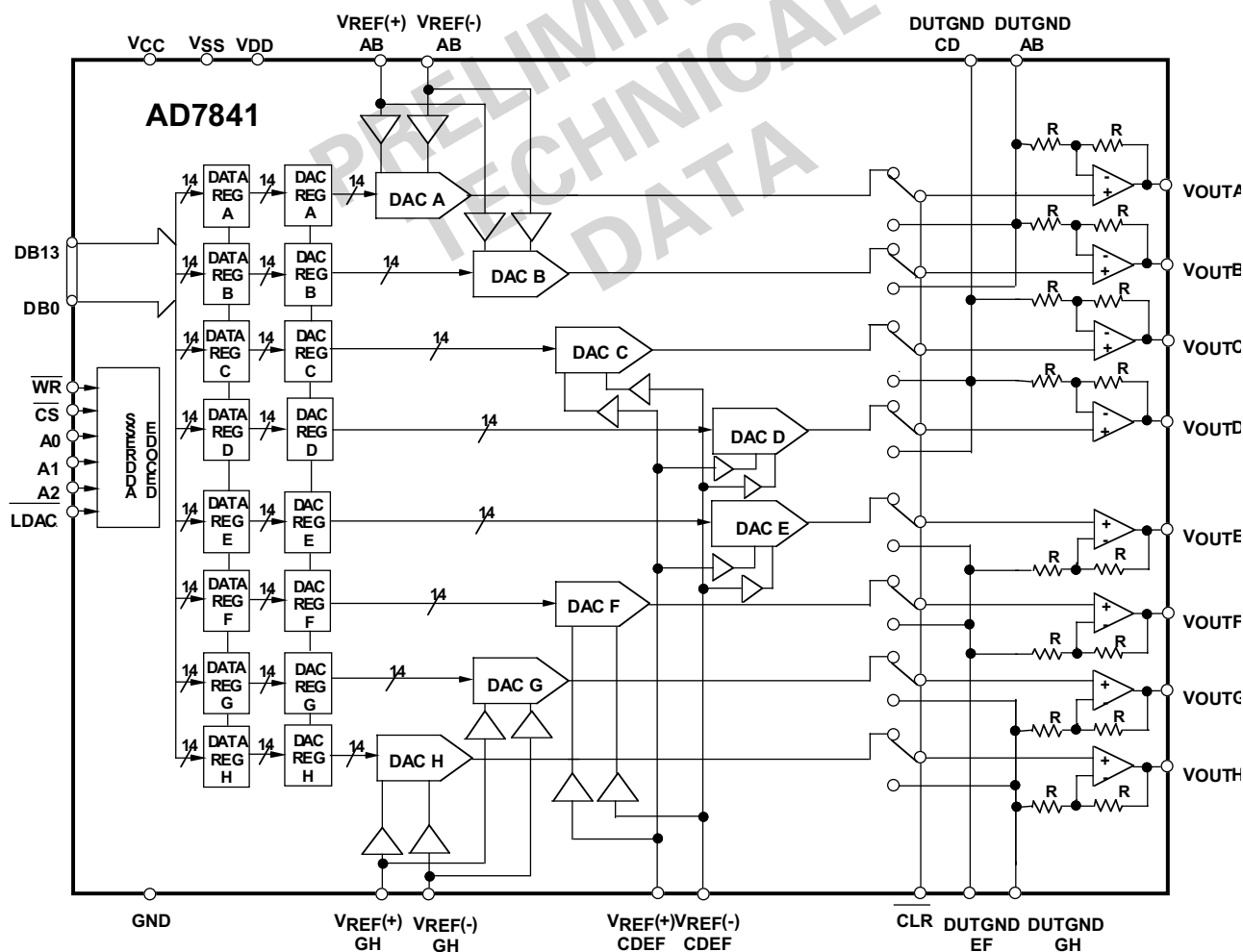
The AD7841 accepts 14-bit parallel loaded data from the external bus into one of the input latches under the control of the  $\overline{WR}$ ,  $\overline{CS}$  and DAC channel address pins, A0–A2.

The DAC outputs are updated on reception of new data into the DAC registers. All the outputs may be updated simultaneously by taking the  $\overline{LDAC}$  input low.

Each DAC output is buffered with a gain-of-two amplifier into which an external DAC offset voltage can be inserted via the DUTGNDx pins.

The AD7841 is available in a 44-pin PQFP package.

### FUNCTIONAL BLOCK DIAGRAM



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# AD7841—SPECIFICATIONS

( $V_{CC} = +5\text{ V} \pm 5\%$ ;  $V_{DD} = +10.8\text{ V to } +16.5\text{ V}$ ;  $V_{SS} = -10.8\text{ V to } -16.5\text{ V}$ ;  $GND = DUTGND = 0\text{ V}$ ;  $R_L = 5\text{ k}\Omega$  and  $C_L = 50\text{ pF}$  to  $GND$ ,  $T_A^1 = T_{MIN}$  to  $T_{MAX}$ , unless otherwise noted)

Parameter	A	B	Units	Test Conditions/Comments
<b>ACCURACY</b>				
Resolution	14	14	Bits	Guaranteed Monotonic Over Temperature $V_{REF}(+) = +5\text{ V}$ , $V_{REF}(-) = -5\text{ V}$ . Typically within $\pm 2\text{ LSB}$ $V_{REF}(+) = +5\text{ V}$ , $V_{REF}(-) = -5\text{ V}$ . Typically within $\pm 2\text{ LSB}$ $V_{REF}(+) = +5\text{ V}$ , $V_{REF}(-) = -5\text{ V}$
Relative Accuracy	$\pm 4$	$\pm 2$	LSB max	
Differential Nonlinearity	$\pm 1$	$\pm 1$	LSB max	
Zero-Scale Error	$\pm 8$	$\pm 4$	LSB max	
Full-Scale Error	$\pm 8$	$\pm 4$	LSB max	
Gain Error	$\pm 4$	$\pm 2$	LSB typ	
Gain Temperature Coefficient <sup>2</sup>	0.5	0.5	ppm FSR/ $^{\circ}\text{C}$ typ	
	10	10	ppm FSR/ $^{\circ}\text{C}$ max	
DC Crosstalk <sup>2</sup>	0.2	0.2	mV max	See Terminology. $R_L = 5\text{ k}\Omega$ , $C_L = 50\text{ pF}$
	0.08	0.08	mV typ	
<b>REFERENCE INPUTS<sup>2</sup></b>				
DC Input Resistance	100	100	M $\Omega$ typ	Per Input. Typically $\pm 50\text{ nA}$
Input Current	$\pm 1$	$\pm 1$	$\mu\text{A}$ max	
$V_{REF}(+)$ Range	0/+5	0/+5	V min/max	For Specified Performance. Can Go as Low as 0 V, but Performance Not Guaranteed
$V_{REF}(-)$ Range	-5/0	-5/0	V min/max	
$[V_{REF}(+) - V_{REF}(-)]$	+2/+10	+2/+10	V min/max	
<b>DUTGND INPUTS<sup>2</sup></b>				
DC Input Impedance	60	60	k $\Omega$ typ	Per Input.
Max Input Current	$\pm 0.3$	$\pm 0.3$	mA typ	
Input Range	-2/+2	-2/+2	V min/max	
<b>OUTPUT CHARACTERISTICS<sup>2</sup></b>				
Output Voltage Swing	$\pm 10$	$\pm 10$	V min	$2 \times (V_{REF}(-) + [V_{REF}(+) - V_{REF}(-)] \cdot D) - V_{DUTGND}$ To 0 V To 0 V
Short Circuit Current	15	15	mA max	
Resistive Load	5	5	k $\Omega$ min	
Capacitive Load	50	50	pF max	
DC Output Impedance	0.5	0.5	$\Omega$ max	
<b>DIGITAL INPUTS</b>				
$V_{INH}$ , Input High Voltage	2.4	2.4	V min	Total of All Digital Pins
$V_{INL}$ , Input Low Voltage	0.8	0.8	V max	
$I_{INH}$ , Input Current	$\pm 10$	$\pm 10$	$\mu\text{A}$ max	
$C_{IN}$ , Input Capacitance <sup>2</sup>	10	10	pF max	
<b>POWER REQUIREMENTS</b>				
$V_{CC}$	+4.75/+5.25	+4.75/+5.25	V min/max	For Specified Performance
$V_{DD}$	+10.8/+16.5	+10.8/+16.5	V min/max	For Specified Performance
$V_{SS}$	-10.8/-16.5	-10.8/-16.5	V min/max	For Specified Performance
Power Supply Sensitivity				
$\Delta\text{Full Scale}/\Delta V_{DD}$	80	80	dB typ	$V_{INH} = V_{CC}$ , $V_{INL} = GND$ . Dynamic Current Outputs Unloaded. Typically 7 mA Outputs Unloaded. Typically 7 mA
$\Delta\text{Full Scale}/\Delta V_{SS}$	80	80	dB typ	
$I_{CC}$	0.5	0.5	mA max	
$I_{DD}$	14	14	mA max	
$I_{SS}$	14	14	mA max	

## NOTES

<sup>1</sup>Temperature range for A and B Versions:  $-40^{\circ}\text{C}$  to  $+85^{\circ}\text{C}$

<sup>2</sup>Guaranteed by characterization. Not production tested.

Specifications subject to change without notice.

# AD7841 Prelim Technical Information

## AC PERFORMANCE CHARACTERISTICS (These characteristics are included for Design Guidance and are not subject to production testing.)

Parameter	A	B	Units	Test Conditions/Comments
<b>DYNAMIC PERFORMANCE</b>				
Output Voltage Settling Time	30	30	$\mu\text{s}$ typ	Full-Scale Change to $\pm 1/2$ LSB. DAC Latch Contents Alternately Loaded with All 0s and All 1s
Slew Rate	0.8	0.8	$\text{V}/\mu\text{s}$ typ	
Digital-to-Analog Glitch Impulse	120	120	$\text{nV-s}$ typ	Measured with $V_{\text{REF}}(+)=+5\text{ V}$ , $V_{\text{REF}}(-)=-5\text{ V}$ . DAC Latch Alternately Loaded with 0FFF Hex and 1000 Hex. Not Dependent on Load Conditions
Channel-to-Channel Isolation	100	100	$\text{dB}$ typ	See Terminology
DAC-to-DAC Crosstalk	5	5	$\text{nV-s}$ typ	See Terminology
Digital Crosstalk	3	3	$\text{nV-s}$ typ	Feedthrough to DAC Output Under Test Due to Change in Digital Input Code to Another Converter
Digital Feedthrough	0.5	0.5	$\text{nV-s}$ typ	Effect of Input Bus Activity on DAC Output Under Test
Output Noise Spectral Density @ 1 kHz	130	130	$\text{nV}/(\text{Hz})^{1/2}$ typ	All 1s Loaded to DAC. $V_{\text{REF}}(+)=V_{\text{REF}}(-)=0\text{ V}$

Specifications subject to change without notice.

## TIMING SPECIFICATIONS<sup>1</sup> ( $V_{\text{CC}} = +5\text{ V} \pm 5\%$ ; $V_{\text{DD}} = +10.8\text{ V}$ to $+16.5\text{ V}$ ; $V_{\text{SS}} = -10.8\text{ V}$ to $-16.5\text{ V}$ ; $\text{GND} = \text{DUTGND} = 0\text{ V}$ )

Parameter	Limit at $T_{\text{MIN}}$ , $T_{\text{MAX}}$	Units	Description
$t_1$	15	ns min	Address to $\overline{\text{WR}}$ Setup Time
$t_2$	0	ns min	Address to $\overline{\text{WR}}$ Hold Time
$t_3$	50	ns min	$\overline{\text{CS}}$ Pulse Width Low
$t_4$	50	ns min	$\overline{\text{WR}}$ Pulse Width Low
$t_5$	0	ns min	$\overline{\text{CS}}$ to $\overline{\text{WR}}$ Setup Time
$t_6$	0	ns min	$\overline{\text{WR}}$ to $\overline{\text{CS}}$ Hold Time
$t_7$	20	ns min	Data Setup Time
$t_8$	0	ns min	Data Hold Time
$t_9$	20	$\mu\text{s}$ typ	Settling Time
$t_{10}$	300	ns max	$\overline{\text{CLR}}$ Pulse Activation Time
$t_{11}$	50	ns min	$\overline{\text{LDAC}}$ Pulse Width Low

### NOTES

<sup>1</sup>All input signals are specified with  $t_r = t_f = 5\text{ ns}$  (10% to 90% of 5 V) and timed from a voltage level of 1.6 V.

<sup>2</sup>Rise and fall times should be no longer than 50 ns.

Specifications subject to change without notice.

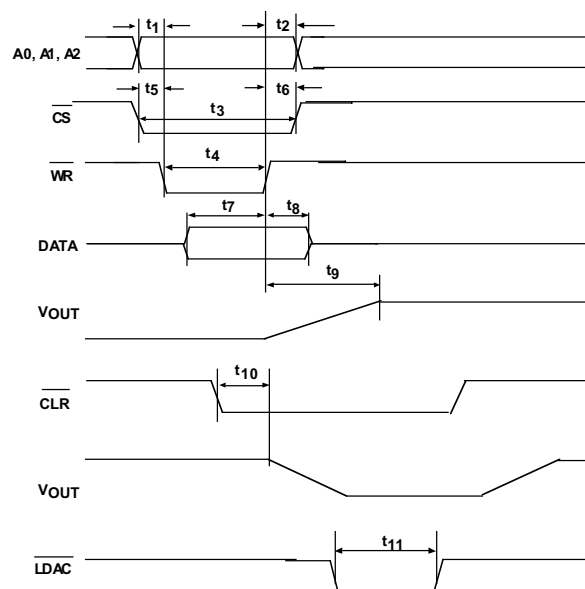


Figure 1. Timing Diagram

# AD7841 Prelim Technical Information

## ABSOLUTE MAXIMUM RATINGS<sup>1</sup>

(T<sub>A</sub> = +25°C unless otherwise noted)

V <sub>CC</sub> to GND	-0.3 V, +7 V or V <sub>DD</sub> + 0.3 V (Whichever Is Lower)
V <sub>DD</sub> to GND	-0.3 V, +17 V
V <sub>SS</sub> to GND	+0.3 V, -17 V
Digital Inputs to GND	-0.3 V, V <sub>CC</sub> + 0.3 V
V <sub>REF</sub> (+) to V <sub>REF</sub> (-)	-0.3 V, +18 V
V <sub>REF</sub> (+) to GND	V <sub>SS</sub> - 0.3 V, V <sub>DD</sub> + 0.3 V
V <sub>REF</sub> (-) to GND	V <sub>SS</sub> - 0.3 V, V <sub>DD</sub> + 0.3 V
DUTGND to GND	V <sub>SS</sub> - 0.3 V, V <sub>DD</sub> + 0.3 V
V <sub>OUT</sub> (A-H) to GND	V <sub>SS</sub> - 0.3 V, V <sub>DD</sub> + 0.3 V
Operating Temperature Range	
Industrial (A, B Versions)	-40°C to +85°C
Storage Temperature Range	-65°C to +150°C
Junction Temperature	+150°C
PQFP Package, Power Dissipation	480 mW

θ <sub>JA</sub> Thermal Impedance	95°C/W
Lead Temperature, Soldering	
Vapor Phase (60 sec)	+215°C
Infrared (15 sec)	+220°C

## NOTES

<sup>1</sup>Stresses above those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

<sup>2</sup>Transient currents of up to 100 mA will not cause SCR latch-up.

## ORDERING GUIDE

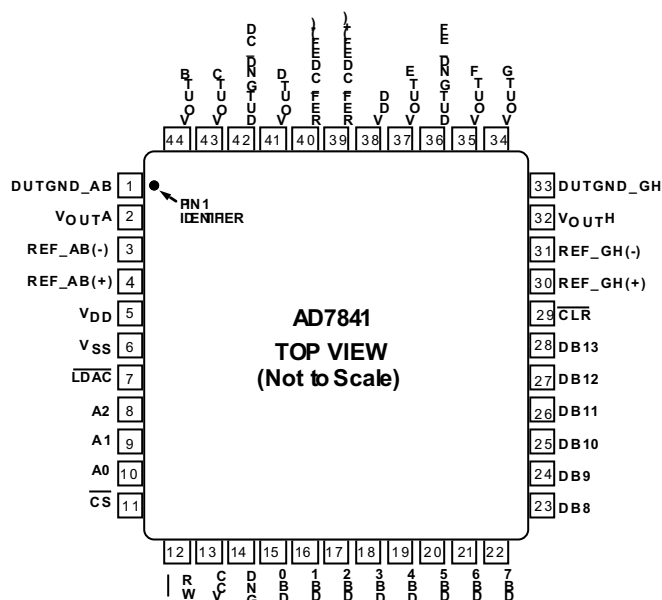
Model	Temperature Range	Linearity Error (LSBs)	DNL (LSBs)	Package Option*
AD7841AS	-40°C to +85°C	±4	±1	S-44
AD7841BS	-40°C to +85°C	±2	±1	S-44

\*S = Plastic Quad Flatpack (PQFP).

## CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although the AD7841 features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.

## PIN CONFIGURATION



# AD7841 Prelim Technical Information

## PIN DESCRIPTION

Pin Mnemonic	Description
V <sub>CC</sub>	Logic Power Supply; +4.75V to +5.25V.
V <sub>SS</sub>	Negative Analog Power Supply; -10.8V to -16.5 V.
V <sub>DD</sub>	Positive Analog Power Supply; +10.8V to +16.5V.
GND	Ground.
V <sub>REF</sub> (+)AB, V <sub>REF</sub> (-)AB	Reference Inputs for DACs A and B. These reference voltages are referred to GND.
V <sub>REF</sub> (+)CDEF, V <sub>REF</sub> (-)CDEF	Reference Inputs for DACs C, D, E and F. These reference voltages are referred to GND.
V <sub>REF</sub> (+)GH, V <sub>REF</sub> (-)GH	Reference Inputs for DACs G and H. These reference voltages are referred to GND.
V <sub>OUT</sub> A . . V <sub>OUT</sub> H	DAC Outputs.
$\overline{\text{CS}}$	Level-Triggered Chip Select Input (active low). The device is selected when this input is low.
DB0 . . DB13	Parallel Data Inputs. The AD7841 can accept a straight 14-bit parallel word on DB0 to DB13 where DB13 is the MSB and DB0 is the LSB.
A0, A1, A2	Address inputs. A0, A1 and A2 are decoded to select one of the eight input data registers for a data transfer.
$\overline{\text{LDAC}}$	Load DAC Logic Input (active low). When this logic input is taken low the contents of the input latches are transferred to their respective DAC latches.
$\overline{\text{CLR}}$	Asynchronous Clear Input (level sensitive, active low). When this input is low, all analog outputs are switched to the externally set potential on the relevant DUTGND pin. The contents of data registers and DAC registers A to H are not affected when the CLR pin is taken low. When CLR is brought back high, the DAC outputs revert back to their original outputs as determined by the data in their DAC registers.
$\overline{\text{WR}}$	Level-Triggered Write Input (active low), used in conjunction with $\overline{\text{CS}}$ to write data to the AD7841 input data registers. Data is latched into the selected data register on the rising edge of $\overline{\text{WR}}$ .
DUTGNDAB	Device Sense Ground for DACs A and B. Vout A and Vout B are referenced to the voltage applied to this pin.
DUTGND CD	Device Sense Ground for DACs C and D. Vout C and Vout D are referenced to the voltage applied to this pin.
DUTGNDEF	Device Sense Ground for DACs E and F. Vout E and Vout F are referenced to the voltage applied to this pin.
DUTGND GH	Device Sense Ground for DACs G and H. Vout G and Vout H are referenced to the voltage applied to this pin.

## OUTLINE DIMENSIONS

Dimensions shown in inches and (mm).

### 44-Pin PQFP (S-44)

