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List of 7400-series integrated circuits

The following is a **list of 7400-series digital logic integrated circuits**. In the mid-1960s, the original 7400series integrated circuits were introduced by <u>Texas Instruments</u> with the prefix "SN" to create the name SN74xx. Due to the popularity of these parts, other manufacturers released pin-to-pin compatible <u>logic</u> devices and kept the 7400 sequence number as an aid to identification of compatible parts. However, other manufacturers use different prefixes and suffixes on their part numbers.

Overview

Some TTL logic parts were made with an extended military-specification temperature range. These parts are prefixed with **54** instead of **74** in the part number. [1]

A short-lived **64** prefix on Texas Instruments parts indicated an industrial temperature range; this prefix had been dropped from the TI literature by 1973. Most recent 7400-series parts are fabricated in <u>CMOS</u> or <u>BiCMOS</u> technology rather than TTL. Surface-mount parts with a single gate (often in a 5-pin or 6-pin package) are prefixed with **741G** instead of **74**.

Some manufacturers released some <u>4000-series</u> equivalent CMOS circuits with a 74 prefix, for example, the 74HC4066^[2] was a replacement for the 4066 with slightly different electrical characteristics (different power-supply voltage ratings, higher frequency capabilities, lower "on" resistances in analog switches, etc.). See List of 4000-series integrated circuits. Conversely, the 4000-series has "borrowed" from the 7400 series – such as the CD40193 and CD40161 being pin-for-pin *functional* replacements for 74C193 and 74C161.

Older TTL parts made by manufacturers such as <u>Signetics</u>, <u>Motorola</u>, <u>Mullard</u> and <u>Siemens</u> may have different numeric prefix and numbering series entirely, such as in the European FJ family FJH101 is an 8-input <u>NAND gate</u> like a 7430.

A few alphabetic characters to designate a specific logic subfamily may immediately follow the **74** or **54** in the part number, e.g., 74LS74 for low-power <u>Schottky</u>. Some CMOS parts such as 74HCT74 for high-speed <u>CMOS</u> with TTL-compatible input thresholds are functionally similar to the TTL part. Not all functions are available in all families. The generic descriptive feature of these alphabetic characters was diluted by various companies participating in the market at its peak and are not always consistent especially with more recent offerings. The National Semiconductor trademarks of the words $FAST^{[3]}$ and $FACT^{[4]}$ are usually cited in the descriptions from other companies when describing their own unique designations.^{[5][6]}

In a few instances, such as the 7478 and 74107, the same suffix in different families do not have completely equivalent logic functions.

Another extension to the series is the **7416xxx** variant, representing mostly the 16-bit-wide counterpart of otherwise 8-bit-wide "base" chips with the same three ending digits. Thus e.g. a "7416373" would be the 16-bit-wide equivalent of a "74373". Some 7416xxx parts, however, do not have a direct counterpart from

the standard 74xxx range but deliver new functionality instead, which needs making use of the 7416xxx series' higher pin count. For more details, refer primarily to the Texas Instruments documentation mentioned in the <u>References</u> section.

For CMOS (AC, HC, etc.) subfamilies, read "open drain" for "open collector" in the table below.

There are a few numeric suffixes that have multiple conflicting assignments, such as the 74453.

Logic gates

Since there are numerous 7400-series parts, the following groups related parts to make it easier to pick a useful part number. This section only includes combinational logic gates.

For part numbers in this section, "x" is the <u>7400-series logic family</u>, such as LS, ALS, HCT, AHCT, HC, AHC, LVC, ...

Normal inputs / push-pull outputs

Configuration	Buffer	Inverter
Hex 1-input	74x34	74x04



Schematic of 74LS51 IC consists of a 3-3 AOI gate and 2-2 AOI gate. AOI means <u>AND-OR-Invert</u> (AND-NOR). Most AOI chips are currently obsolete.



74LS51 pinout diagram

Configuration	AND	NAND	OR	NOR	XOR	XNOR
Quad 2-input	74x08	74x00	74x32	74x02	74x86	74x7266
Triple 3-Input	74x11	74x10	74x4075	74x27	n/a	n/a
Dual 4-input	74x21	74x20	74x4072	74x29	n/a	n/a
Single 8-input	n/a	74x30	74x4078	74x4078	n/a	n/a

Schmitt-trigger inputs / push-pull outputs

Configuration	Buffer	Inverter		
Hex 1-input	74x7014	74x14		
Configuration	AND	NAND	OR	NOR
Ouad 2-input	7/1×7001	7/y132	7/x7032	74x7002
C	14/1001	14/102	14/1002	14/1002



TI SN74LS51 in DIP-14 package

Normal inputs / open-collector outputs

Configuration	Buffer	Inverter		
Hex 1-input	74x07	74x05		

Configuration	AND	NAND	OR	NOR	XOR	XNOR
Quad 2-input	74x09	74x03	n/a	74x33	74x136	74x266
Triple 3-input	74x15	74x12	n/a	n/a	n/a	n/a
Dual 4-input	n/a	74x22	n/a	n/a	n/a	n/a

Schmitt-trigger inputs / three-state outputs

Configuration	Buffer	Inverter
Octal 1-input	74x241 74x244	74x240

AND-OR-invert (AOI) logic gates

NOTE: in past decades, a number of <u>AND-OR-invert</u> (AOI) parts were available in 7400 TTL families, but currently most are obsolete.

- SN5450 = dual 2-2 AOI gate, one is expandable (SN54 is military version of SN74)
- SN74LS51 = 2-2 AOI gate and 3-3 AOI gate
- SN54LS54 = single 2-3-3-2 AOI gate

Larger footprints

Parts in this section have a pin count of 14 pins or more. The lower part numbers were established in the 1960s and 1970s, then higher part numbers were added incrementally over decades. IC manufacturers continue to make a core subset of this group, but many of these part numbers are considered obsolete and no longer manufactured. Older discontinued parts may be available from a limited number of sellers as <u>new</u> old stock (NOS), though some are much harder to find.

For the following table:

- Part number column the "x" is a place holder for the logic subfamily name. For example, 74x00 in "LS" logic family would be "74LS00".
- Description column simplified to make it easier to sort, thus isn't identical to datasheet title. The terms Schmitt trigger, open-collector/open-drain, three-state were moved to the input and output columns to make it easier to sort by those features.

- Input column a blank cell means a normal input for the logic family type.
- Output column a blank cell means a "totem pole" output, also known as a <u>push-pull output</u>, with the ability to drive ten standard inputs of the same logic subfamily (<u>fan-out</u> N_O = 10). Outputs with higher output currents are often called drivers or buffers.
- Pins column number of pins for the <u>dual in-line package</u> (DIP) version; a number in <u>parentheses</u> (round brackets) indicates that there is no known dual in-line package version of this IC.

Part number	Units	Description	Input	Output	Pins	Datasheet
74x00	4	quad 2-input NAND gate			14	SN74LS00 (http://www.t i.com/lit/gpn/sn74ls00)
74x01	4	quad 2-input NAND gate; different pinout for 74H01		open- collector	14	SN74LS01 (https://archive.org/details/bitsavers_ tidataBookVol2_4594535 2/page/n61/)
74x02	4	quad 2-input NOR gate			14	SN74LS02 (http://www.t i.com/lit/gpn/sn74ls02)
74x03	4	quad 2-input NAND gate		open- collector	14	SN74LS03 (http://www.t i.com/lit/gpn/sn54ls03)
74x04	6	hex inverter gate			14	SN74LS04 (http://www.t i.com/lit/gpn/sn74ls04)
74x05	6	hex inverter gate		open- collector	14	SN74LS05 (http://www.t i.com/lit/gpn/sn74ls05)
74x06	6	hex inverter gate		open- collector 30 V / 40 mA	14	SN74LS06 (http://www.t i.com/lit/gpn/sn74ls06)
74x07	6	hex buffer gate		open- collector 30 V / 40 mA	14	SN74LS07 (http://www.t i.com/lit/gpn/sn74ls07)
74x08	4	quad 2-input AND gate			14	SN74LS08 (http://www.t i.com/lit/gpn/sn74ls08)
74x09	4	quad 2-input AND gate		open- collector	14	SN74LS09 (http://www.t i.com/lit/gpn/sn74ls09)
74x10	3	triple 3-input NAND gate			14	SN74LS10 (http://www.t i.com/lit/gpn/sn74ls10)
74x11	3	triple 3-input AND gate			14	SN74LS11 (http://www.t i.com/lit/gpn/sn74ls11)
74x12	3	triple 3-input NAND gate		open- collector	14	SN74LS12 (http://pdf.dat asheetcatalog.com/data sheet/motorola/SN54LS 12J.pdf)
74x13	2	dual 4-input NAND gate	Schmitt trigger		14	SN74LS13 (https://archive.org/details/bitsavers_ tidataBookVol2_4594535 2/page/n125)
74x14	6	hex inverter gate	Schmitt trigger		14	SN74LS14 (http://www.t i.com/lit/gpn/sn74ls14)
74x15	3	triple 3-input AND gate		open- collector	14	SN74LS15 (http://pdf.dat asheetcatalog.com/data sheet/motorola/74LS15. pdf)
74x16	6	hex inverter gate		open- collector 15 V / 40 mA	14	SN7416 (http://www.ti.co m/lit/gpn/sn7416)
74x17	6	hex buffer gate		open- collector	14	SN7417 (http://www.ti.co m/lit/gpn/sn7417)

				15 V / 40 mA		
74x18	2	dual 4-input NAND gate	Schmitt trigger		14	SN74LS18 (https://archi ve.org/details/bitsavers_ tidataBookVol2_4594535 2/page/n149)
74x19	6	hex inverter gate	Schmitt trigger		14	SN74LS19 (https://archi ve.org/details/bitsavers_ tidataBookVol2_4594535 2/page/n149)
74x20	2	dual 4-input NAND gate			14	SN74LS20 (http://www.t i.com/lit/gpn/sn74ls20)
74x21	2	dual 4-input AND gate			14	SN74LS21 (http://www.t i.com/lit/gpn/sn74ls21)
74x22	2	dual 4-input NAND gate		open- collector	14	SN74LS22 (http://pdf.dat asheetcatalog.com/data sheets/270/331402_DS. pdf)
74x23	2	dual 4-input NOR gate with strobe, one gate expandable with 74x60			16	SN7423 (http://www.ti.co m/lit/gpn/sn5423)
74x24	4	quad 2-input NAND gate	Schmitt trigger		14	SN74LS24 (https://archi ve.org/details/bitsavers_ tidataBookVol2_4594535 2/page/n149)
74x25	2	dual 4-input NOR gate with strobe			14	SN7425 (http://www.ti.co m/lit/gpn/sn7425)
74x26	4	quad 2-input NAND gate		open- collector 15 V	14	SN74LS26 (http://www.t i.com/lit/gpn/sn74ls26)
74x27	3	triple 3-input NOR gate			14	SN74LS27 (http://www.t i.com/lit/gpn/sn74ls27)
74x28	4	quad 2-input NOR gate		driver N _O =30	14	SN74LS28 (http://www.t i.com/lit/gpn/sn5428)
74x29	2	dual 4-input NOR gate			14	US7429A (https://archiv e.org/stream/bitsavers_d erivationates1974Digitall ntegratedCircuitDataBoo k_79049866#page/n101)
74x30	1	single 8-input NAND gate			14	SN74LS30 (http://www.t i.com/lit/gpn/sn74ls30)
74x31	6	hex delay elements (two 6ns, two 23-32ns, two 45- 48ns)			16	SN74LS31 (http://www.t i.com/lit/gpn/sn74ls31)
74x32	4	quad 2-input OR gate			14	SN74LS32 (http://www.t i.com/lit/gpn/sn74ls32)
74x33	4	quad 2-input NOR gate		open- collector driver N _O =30	14	SN74LS33 (http://www.t i.com/lit/gpn/sn74ls33)
74x34	6	hex buffer gate			14	MM74HC34 (http://pdf.d

					asheet/nationalsemicond uctor/DS009389.PDF)
74x35	6	hex buffer gate	open- collector	14	SN74ALS35 (https://arc hive.org/details/bitsaver s_tidataBookVol3_25840 031/page/n101)
74x36	4	quad 2-input NOR gate (different pinout than 7402)		14	SN74HC36 (https://archi ve.org/details/bitsavers_ tidataBookogicDataBook _23574286/page/n81)
74x37	4	quad 2-input NAND gate	driver N _O =30	14	SN74LS37 (http://www.t i.com/lit/gpn/sn74ls37)
74x38	4	quad 2-input NAND gate	open- collector driver N _O =30	14	SN74LS38 (http://www.t i.com/lit/gpn/sn74ls38)
74x39	4	quad 2-input NAND gate (different <u>pinout</u> than 7438)	open- collector 60 mA	14	SN7439 (http://pdf.datas heetcatalog.com/datash eets/90/338005_DS.pdf)
74x40	2	dual 4-input NAND gate	driver N _O =30	14	SN74LS40 (http://pdf.dat asheetcatalog.com/data sheet/motorola/SN54LS 40J.pdf)
74x41	1	BCD to decimal decoder / Nixie tube driver	open- collector 70 V	16	DM7441A (https://archiv e.org/details/bitsavers_n ationaldaTTLDatabook_4 2712617/page/n146)
74x42	1	BCD to decimal decoder		16	SN74LS42 (http://www.t i.com/lit/gpn/sn74ls42)
74x43	1	excess-3 to decimal decoder		16	SN7443A (https://archiv e.org/details/bitsavers_ti dataBookVol2_4594535 2/page/n231)
74x44	1	Gray code to decimal decoder		16	SN7444A (https://archiv e.org/details/bitsavers_ti dataBookVol2_4594535 2/page/n231)
74x45	1	BCD to decimal decoder/driver	open- collector 30 V / 80 mA	16	SN7445 (http://www.ti.co m/lit/gpn/sn7445)
74x46	1	BCD to <u>7-segment display</u> decoder/driver	open- collector 30 V	16	SN7446A (https://archiv e.org/details/bitsavers_ti dataBookVol2_4594535 2/page/n244)
74x47	1	BCD to 7-segment decoder/driver	open- collector 15 V	16	SN74LS47 (http://www.t i.com/lit/gpn/sn74ls47)
74x48	1	BCD to 7-segment decoder/driver	open- collector, 2 kΩ pull-up	16	SN74LS48 (https://archive.org/details/bitsavers_ tidataBookVol2_4594535 2/page/n244)
74x49	1	BCD to 7-segment decoder/driver	open- collector	14	SN74LS49 (https://archive.org/details/bitsavers_

					tidataBookVol2_4594535 2/page/n244)
74x50	2	dual 2-2-input AND-OR-Invert gate, one gate expandable		14	SN7450 (http://www.ti.co m/lit/gpn/sn5450)
7451, 74H51, 74S51	2	dual 2-2-input AND-OR-Invert (AOI) gate		14	SN7451 (http://www.ti.co m/lit/gpn/sn74ls51)
74L51, 74LS51	2	3-3-input AND-OR-Invert gate and 2-2-input AND-OR-Invert gate		14	SN74LS51 (http://www.t i.com/lit/gpn/sn74ls51)
74x52	1	3-2-2-2-input AND-OR gate, expandable with 74x61		14	SN74H52 (https://archiv e.org/details/bitsavers_ti dataBookVol2_4594535 2/page/n271)
7453	1	2-2-2-2-input AND-OR-Invert gate, expandable		14	SN7453 (https://archive. org/details/bitsavers_tid ataBookVol2_45945352/ page/n273)
74H53	1	3-2-2-2-input AND-OR-Invert gate, expandable		14	SN74H53 (https://archiv e.org/details/bitsavers_ti dataBookVol2_4594535 2/page/n273)
7454	1	2-2-2-2-input AND-OR-Invert gate		14	SN7454 (http://www.ti.co m/lit/gpn/sn5454)
74H54	1	3-2-2-2-input AND-OR-Invert gate		14	SN74H54 (https://archiv e.org/details/bitsavers_ti dataBookVol2_4594535 2/page/n279)
74L54, 74LS54	1	3-3-2-2-input AND-OR-Invert gate		14	SN74LS54 (http://www.t i.com/lit/gpn/sn5454)
74x55	1	4-4-input AND-OR-Invert gate, 74H55 is expandable		14	SN74LS55 (https://archi ve.org/details/bitsavers_ tidataBookVol2_4594535 2/page/n287)
74x56	1	50:1 frequency divider		8	SN74LS56 (https://archi ve.org/details/bitsavers_ tidataBookVol2_4594535 2/page/n291)
74x57	1	60:1 frequency divider		8	SN74LS57 (https://archive.org/details/bitsavers_ tidataBookVol2_4594535 2/page/n291)
74x58	2	3-3-input AND-OR gate and 2-2-input AND-OR gate		14	74HC58 (https://media.di gikey.com/pdf/Data%20 Sheets/NXP%20PDFs/7 4HC58.pdf)
74x59	2	dual 3-2-input AND-OR-Invert gate		14	US7459A (https://archiv e.org/stream/bitsavers_d erivationates1974Digitall ntegratedCircuitDataBoo k_79049866#page/n103)
74x60	2	dual 4-input expander for 74x23, 74x50, 74x53, 74x55		14	SN7460 (http://pdf.datas heetcatalog.com/datash eets/166/501736_DS.pd f)

74x61	3	triple 3-input expander for 74x52		14	SN74H61 (https://archiv e.org/details/bitsavers_ti dataBookVol2_4594535 2/page/n299)
74x62	1	3-3-2-2-input AND-OR expander for 74x50, 74x53, 74x55		14	SN74H62 (https://archiv e.org/details/bitsavers_ti dataBookVol2_4594535 2/page/n301)
74x63	6	hex current sensing interface gates		14	SN74LS63 (https://archi ve.org/details/bitsavers_ tidataBookVol2_4594535 2/page/n303)
74x64	1	4-3-2-2-input AND-OR-Invert gate		14	SN74S64 (http://www.ti. com/lit/gpn/sn54s64)
74x65	1	4-3-2-2 input AND-OR-Invert gate	open- collector	14	SN74S65 (http://www.ti. com/lit/gpn/sn54s64)
74x67	1	AND gated J-K master-slave flip-flop, asynchronous preset and clear (improved 74L72)		(16)	BL54L67Y (https://ntrs.n asa.gov/archive/nasa/ca si.ntrs.nasa.gov/197200 20596.pdf)
74L68	2	dual J-K flip-flop, asynchronous clear (improved 74L73)		(18)	BL54L68Y (https://ntrs.n asa.gov/archive/nasa/ca si.ntrs.nasa.gov/197200 20596.pdf)
74LS68	2	dual 4-bit decade counters		16	SN74LS68 (https://archi ve.org/details/bitsavers_ tidataBookVol2_4594535 2/page/n311)
74L69	2	dual J-K flip-flop, asynchronous preset, common clock and clear		(18)	BL54L69Y (https://archiv e.org/stream/bitsavers_d erivationates1974Digitall ntegratedCircuitDataBoo k_79049866#page/n47)
74LS69	2	dual 4-bit binary counters		16	SN74LS69 (https://archive.org/details/bitsavers_ tidataBookVol2_4594535 2/page/n311)
74x70	1	AND-gated positive edge triggered J-K flip-flop, asynchronous preset and clear		14	SN7470 (https://archive. org/details/bitsavers_tid ataBookVol2_45945352/ page/n317)
74H71	1	AND-OR-gated J-K master- slave flip-flop, preset		14	SN74H71 (https://archiv e.org/details/bitsavers_ti dataBookVol2_4594535 2/page/n321)
74L71	1	AND-gated R-S master-slave flip-flop, preset and clear		14	SN54L71 (https://archiv e.org/details/bitsavers_ti dataBookVol2_4594535 2/page/n325)
74x72	1	AND gated J-K master-slave flip-flop, asynchronous preset and clear		14	SN7472 (http://www.ti.co m/lit/gpn/sn5472)
74x73	2	dual J-K flip-flop, asynchronous clear		14	SN54LS73A (http://www. ti.com/lit/gpn/sn54ls73a)

74x74	2	dual D positive edge triggered flip-flop, asynchronous preset and clear		14	SN74LS74A (http://www. ti.com/lit/gpn/sn74ls74a)
74x75	2	4-bit bistable latch, complementary outputs		16	SN74LS75 (http://www.t i.com/lit/gpn/sn74ls75)
74x76	2	dual J-K flip-flop, asynchronous preset and clear		16	SN74LS76A (http://www. ti.com/lit/gpn/sn54ls76a)
74x77	1	4-bit bistable latch		14	SN74LS77 (http://www.t i.com/lit/gpn/sn74ls75)
74H78	2	dual positive pulse triggered J-K flip-flop, preset, common clock and common clear		14	SN74H78 (https://archiv e.org/details/bitsavers_ti dataBookVol2_4594535 2/page/n369)
74L78	2	dual positive pulse triggered J-K flip-flop, preset, common clock and common clear		14	SN54L78 (https://archiv e.org/details/bitsavers_ti dataBookVol2_4594535 2/page/n369)
74LS78	2	dual negative edge triggered J-K flip-flop, preset, common clock and common clear		14	SN74LS78A (https://arch ive.org/details/bitsavers _tidataBookVol2_459453 52/page/n369)
74x79	2	dual D positive edge triggered flip-flop, asynchronous preset and clear		14	MC7479 (https://archive. org/details/bitsavers_mo toroladaTTLIntegratedCir cuitsDataBook_3844285 7/page/n387)
74x80	1	gated <u>full adder</u>		14	SN7480 (https://archive. org/details/bitsavers_tid ataBookVol2_45945352/ page/n377)
74x81	1	16-bit <u>RAM</u>		14	SN7481A (http://datashe et.datasheetarchive.co m/originals/distributors/D atasheets-111/DSAP003 6758.pdf)
74x82	1	2-bit binary full adder		14	SN7482 (https://archive. org/details/bitsavers_tid ataBookVol2_45945352/ page/n379)
74x83	1	4-bit binary full adder		16	SN74LS83A (https://arch ive.org/details/bitsavers _tidataBookVol2_459453 52/page/n383)
74x84	1	16-bit <u>RAM</u>		16	SN7484A (http://datashe et.datasheetarchive.co m/originals/distributors/D atasheets-111/DSAP003 6758.pdf)
74x85	1	4-bit magnitude comparator		16	SN74LS85 (http://www.t i.com/lit/gpn/sn74ls85)
74x86	4	quad 2-input XOR gate		14	SN74LS86A (http://www. ti.com/lit/gpn/sn74ls86a)

74x87	1	4-bit true/complement/zero/one element			14	SN74H87 (https://archiv e.org/details/bitsavers_ti dataBookVol2_4594535 2/page/n403)
74x88	1	256-bit <u>ROM</u> (32x8)		open- collector	16	SN7488A (https://archiv e.org/details/bitsavers_ti dataBookcomputerComp onentsDataBook_16851 665/page/n181)
74x89	1	64-bit <u>RAM</u> (16x4), 4 data inputs, 4 inverted data outputs		open- collector	16	SN7489 (http://pdf.datas heetcatalog.com/datash eets/270/499426_DS.pd f)
74x90	1	decade counter (separate divide-by-2 and divide-by-5 sections)			14	SN74LS90 (http://www.t i.com/lit/gpn/sn74ls90)
74x91	1	8-bit shift register, serial in, serial out, gated input			14	SN74LS91 (https://archi ve.org/details/bitsavers_ tidataBookVol2_4594535 2/page/n419)
74x92	1	divide-by-12 counter (separate divide-by-2 and divide-by-6 sections)			14	SN74LS92 (http://www.t i.com/lit/gpn/sn74ls92)
74x93	1	4-bit binary counter (separate divide-by-2 and divide-by-8 sections); different pinout for 74L93			14	SN74LS93 (https://www. datasheets360.com/pdf/ 7761228217550421319)
74x94	1	4-bit shift register, dual asynchronous presets			16	SN7494 (https://archive. org/details/bitsavers_tid ataBookVol2_45945352/ page/n423)
74x95	1	4-bit shift register, parallel in, parallel out, serial input; different pinout for 74L95			14	SN74LS95B (https://ww w.datasheets360.com/pd f/-505384396674053079 3)
74x96	1	5-bit parallel-in/parallel-out shift register, asynchronous preset			16	SN74LS96 (https://archi ve.org/details/bitsavers_ tidataBookVol2_4594535 2/page/n435)
74x97	1	synchronous 6-bit binary rate multiplier			16	SN7497 (http://www.ti.co m/lit/gpn/sn5497)
74x98	1	4-bit data selector/storage register			16	SN54L98 (https://archiv e.org/details/bitsavers_ti dataBookVol2_4594535 2/page/n449)
74x99	1	4-bit bidirectional universal shift register			16	SN54L99 (https://archiv e.org/details/bitsavers_ti dataBookVol2_4594535 2/page/n451)
Part number	Units	Description	Input	Output	Pins	Datasheet
74x100	2	dual 4-bit bistable latch			24	SN74100 (https://archiv e.org/details/bitsavers_ti dataBookVol2_4594535 2/page/n457)

74x101	1	AND-OR-gated J-K negative- edge-triggered flip-flop, preset		14	SN74H101 (https://archi ve.org/details/bitsavers_ tidataBookVol2_4594535 2/page/n459)
74x102	1	AND-gated J-K negative- edge-triggered flip-flop, preset and clear		14	SN74H102 (https://archi ve.org/details/bitsavers_ tidataBookVol2_4594535 2/page/n463)
74x103	2	dual J-K negative-edge- triggered flip-flop, clear		14	SN74H103 (https://archi ve.org/details/bitsavers_ tidataBookVol2_4594535 2/page/n465)
74x104	1	J-K master-slave flip-flop		14	SN74104 (https://archiv e.org/details/bitsavers_ti dataBookVol2_4594535 2/page/n469)
74x105	1	J-K master-slave flip-flop, J2 and K2 inverted		14	SN74105 (https://archiv e.org/details/bitsavers_ti dataBookVol2_4594535 2/page/n469)
74x106	2	dual J-K negative-edge- triggered flip-flop, preset and clear		16	SN74H106 (https://archi ve.org/details/bitsavers_ tidataBookVol2_4594535 2/page/n471)
74x107	2	dual J-K flip-flop, clear		14	SN74107 (http://www.ti.c om/lit/gpn/sn74ls107a)
74x107A	2	dual J-K negative-edge- triggered flip-flop, clear		14	SN74LS107A (https://we b.archive.org/web/20070 125105009/http://focus.t i.com/lit/ds/symlink/sn7 4107.pdf)
74x108	2	dual J-K negative-edge- triggered flip-flop, preset, common clear and common clock		14	SN74H108 (https://archi ve.org/details/bitsavers_ tidataBookVol2_4594535 2/page/n479)
74x109	2	dual J-NotK positive-edge- triggered flip-flop, clear and preset		16	SN74109 (http://www.ti.c om/lit/gpn/sn74ls109a)
74x110	1	AND-gated J-K master-slave flip-flop, data lockout		14	SN74110 (https://archiv e.org/details/bitsavers_ti dataBookVol2_4594535 2/page/n487)
74x111	2	dual J-K master-slave flip- flop, data lockout, reset, set		16	TL74111N (https://web.a rchive.org/web/20180727 181024/http://www.feceg ypt.com/uploads/dataSh eet/1481104190_tl74115 n.pdf)
74x112	2	dual J-K negative-edge- triggered flip-flop, clear and preset		16	SN74LS112A (http://ww w.ti.com/lit/gpn/sn74s11 2a)
74x113	2	dual J-K negative-edge- triggered flip-flop, preset		14	SN74LS113A (https://arc hive.org/details/bitsaver s_tidataBookVol2_45945 352/page/n499)

74x114	2	dual J-K negative-edge- triggered flip-flop, preset, common clock and clear			14	SN74LS114A (https://arc hive.org/details/bitsaver s_tidataBookVol2_45945 352/page/n505)
74x115	2	dual J-K master-slave flip- flop, data lockout, reset			14	TL74115N (https://web.a rchive.org/web/20180727 181024/http://www.feceg ypt.com/uploads/dataSh eet/1481104190_tl74115 n.pdf)
74116, 74L116	2	dual 4-bit latch, clear			24	SN74116 (https://archiv e.org/details/bitsavers_ti dataBookVol2_4594535 2/page/n511) ^{[7]:1-123}
74H116	1	AND-gated J-K flip flop	?	?	14	MC74H116 (https://archi ve.org/details/Digital_IC _Equivalents/page/n97)
74x117	1	AND-gated J-K flip flop, one J and K input inverted	?	?	14	MC74H117 (https://archi ve.org/details/Digital_IC _Equivalents/page/n97)
74x118	6	hex set/reset latch, common reset			16	ITT74118 (https://archiv e.org/details/bitsavers_it tdataBootorProductCatal og_54440015/page/n16 1)
74119	6	hex set/reset latch			24	TL74119N (https://archiv e.org/stream/bitsavers_d erivationates1974Digitall ntegratedCircuitDataBoo k_79049866#page/n57) [7]:1–125
74H119	2	dual J-K flip-flop, shared clear and clock inputs	?	?	14	MC74H119 (https://archi ve.org/details/Digital_IC _Equivalents/page/n97)
74120	2	dual pulse synchronizer/drivers	15 kΩ pull-up		16	SN74120 (https://archiv e.org/details/bitsavers_ti dataBookVol2_4594535 2/page/n515)
74H120	2	dual J-K flip-flop, separate clock inputs	?	?	14	MC74H120 (https://archi ve.org/details/Digital_IC _Equivalents/page/n97)
74x121	1	monostable multivibrator	Schmitt trigger		14	SN74121 (http://www.ti.c om/lit/gpn/sn74121)
74x122	1	retriggerable monostable multivibrator, clear			14	SN74122 (http://www.ti.c om/lit/gpn/sn74ls122)
74x123	2	dual retriggerable monostable multivibrator, clear			16	SN74123 (http://www.ti.c om/lit/gpn/sn74ls122)
74x124	2	dual voltage-controlled oscillator	analog		16	SN74S124 (http://www.t i.com/lit/gpn/sn54s124)
74x125	4	quad bus buffer, negative enable		three- state	14	SN74LS125A (http://ww w.ti.com/lit/gpn/sn74ls12 6a)

74x126	4	quad bus buffer, positive enable		three- state	14	SN74LS126A (http://ww w.ti.com/lit/gpn/sn74ls12 6a)
74x128	4	quad 2-input NOR gate		driver 50 Ω	14	SN74128 (http://www.ti.c om/lit/gpn/sn74128)
74x130	2	retriggerable monostable multivibrator			16	SN74130 (http://www.ti.c om/lit/gpn/sn74ls122)
74131	4	quad 2-input AND gate		open- collector 15 V	14	ITT74131 (https://archiv e.org/details/bitsavers_it tdataBootorProductCatal og_54440015/page/n18 1)
74AS131, 74ALS131	1	3-to-8 line decoder/demultiplexer, address register, inverting outputs			16	SN74AS131 (https://dat asheet.datasheetarchiv e.com/originals/scans/S cans-067/DSA2IH00211 615.pdf)
74x132	4	quad 2-input NAND gate	Schmitt trigger		14	SN74LS132 (http://www. ti.com/lit/gpn/sn74ls132)
74x133	1	single 13-input NAND gate			16	SN54ALS133 (http://ww w.ti.com/lit/gpn/sn54als1 33)
74x134	1	single 12-input NAND gate		three- state	16	SN74S134 (http://www.t i.com/lit/gpn/sn54s134)
74x135	4	quad XOR/XNOR gate, two inputs to select logic type			16	SN74S135 (https://archi ve.org/details/bitsavers_ tidataBookVol2_4594535 2/page/n567)
74x136	4	quad 2-input XOR gate		open- collector	14	SN74LS136 (http://www. ti.com/lit/gpn/sn74ls136)
74x137	1	3-to-8 line decoder/demultiplexer, address latch, inverting outputs			16	SN74LS137 (https://arch ive.org/details/bitsavers _tidataBookVol2_459453 52/page/n573)
74x138	1	3-to-8 line decoder/demultiplexer, inverting outputs			16	SN74LS138 (http://www. ti.com/lit/gpn/sn74ls138)
74x139	2	dual 2-to-4 line decoder/demultiplexer, inverting outputs			16	SN74LS139A (http://ww w.ti.com/lit/gpn/sn74ls13 9a)
74x140	2	dual 4-input NAND gate		driver 50 Ω	14	SN74S140 (http://www.t i.com/lit/gpn/sn54s140)
74x141	1	BCD to decimal decoder/driver for cold- cathode indicator / Nixie tube		open- collector 60 V	16	DM74141 (https://archiv e.org/details/bitsavers_n ationaldaTTLDatabook_4 2712617/page/n146)
74x142	1	decade counter/latch/decoder/driver for Nixie tubes		open- collector 60 V	16	SN74142 (https://archiv e.org/details/bitsavers_ti dataBook2ed07_233019 73/page/n137)
74x143	1	decade counter/latch/decoder/7- segment driver		constant current 15 mA	24	SN74143 (https://archiv e.org/details/bitsavers_ti

					dataBook2ed07_233019 73/page/n141)
74x144	1	decade counter/latch/decoder/7- segment driver	open- collector 15 V / 25 mA	24	SN74144 (https://archiv e.org/details/bitsavers_ti dataBook2ed07_233019 73/page/n141)
74x145	1	BCD to decimal decoder/driver	open- collector 15 V / 80 mA	16	SN74145 (http://www.ti.c om/lit/gpn/sn74ls145)
74x146	1	3-to-8 line decoder			MCE74H146 (https://arc hive.org/details/bitsaver s_motoroladaTTLIntegra tedCircuitsDataBook_38 442857/page/n77)
74x147	1	10-line to 4-line priority encoder		16	SN74147 (http://www.ti.c om/lit/gpn/sn74ls148)
74x148	1	8-line to 3-line priority encoder		16	SN74148 (http://www.ti.c om/lit/gpn/sn74ls148)
74x149	1	8-line to 8-line priority encoder		20	MM74HCT149 (http://pd f.datasheetcatalog.com/ datasheet/nationalsemic onductor/DS005364.PD F)
74x150	1	16-line to 1-line data selector/multiplexer		24	SN74150 (http://www.ti.c om/lit/gpn/sn74ls151)
74x151	1	8-line to 1-line data selector/multiplexer		16	SN74151A (http://www.ti. com/lit/gpn/sn74ls151)
74x152	1	8-line to 1-line data selector/multiplexer, inverting output		14	SN54152A (https://archi ve.org/details/bitsavers_ tidataBookVol2_4594535 2/page/n611)
74x153	2	dual 4-line to 1-line data selector/multiplexer, non- inverting outputs		16	SN74153 (http://www.ti.c om/lit/gpn/sn74ls153)
74x154	1	4-to-16 line decoder/demultiplexer, inverting outputs		24	SN74154 (https://web.ar chive.org/web/20150321 045049/http://www.ti.co m/lit/ds/symlink/sn7415 4.pdf)
74x155	2	dual 2-to-4 line decoder/demultiplexer, inverting outputs		16	SN74155 (http://www.ti.c om/lit/gpn/sn74ls155a)
74x156	2	dual 2-to-4 line decoder/demultiplexer, inverting outputs	open- collector	16	SN74156 (http://www.ti.c om/lit/gpn/sn74ls155a)
74x157	4	quad 2-line to 1-line data selector/multiplexer, non- inverting outputs		16	SN74157 (http://www.ti.c om/lit/gpn/sn74ls157)
74x158	4	quad 2-line to 1-line data selector/multiplexer, inverting outputs		16	SN74LS158 (http://www. ti.com/lit/gpn/sn74ls157)
74x159	1	4-to-16 line decoder/demultiplexer	open- collector	24	SN74159 (https://web.ar chive.org/web/20070102

					021404/http://focus.ti.co m/lit/ds/symlink/sn7415 9.pdf)
74x160	1	synchronous presettable 4- bit decade counter, asynchronous clear		16	SN74160 (http://www.ti.c om/lit/gpn/sn74ls161a)
74x161	1	synchronous presettable 4- bit binary counter, asynchronous clear		16	SN74161 (http://www.ti.c om/lit/gpn/sn74ls161a)
74x162	1	synchronous presettable 4- bit decade counter, synchronous clear		16	SN74162 (http://www.ti.c om/lit/gpn/sn74ls161a)
74x163	1	synchronous presettable 4- bit binary counter, synchronous clear		16	SN74163 (http://www.ti.c om/lit/gpn/sn74ls161a)
74x164	1	8-bit serial-in parallel-out (SIPO) shift register, asynchronous clear, not output latch		14	SN74164 (http://www.ti.c om/lit/gpn/sn74ls164)
74x165	1	8-bit parallel-in serial-out (PISO) shift register, parallel load, complementary outputs		16	SN74165 (http://www.ti.c om/lit/ds/symlink/sn54h c165.pdf)
74x166	1	parallel-load 8-bit shift register		16	SN74166 (http://www.ti.c om/lit/gpn/sn54ls166a)
74x167	1	synchronous decade rate multiplier		16	SN74167 (https://archiv e.org/details/bitsavers_ti dataBookVol2_4594535 2/page/n695)
74x168	1	synchronous presettable 4- bit up/down decade counter		16	DM74LS168 (https://arc hive.org/details/bitsaver s_nationaldaTTLDataboo k_42712617/page/n229)
74x169	1	synchronous presettable 4- bit up/down binary counter		16	SN74LS169B (http://ww w.ti.com/lit/gpn/sn74ls16 9b)
74x170	1	16-bit register file (4x4)	open- collector	16	SN74170 (https://archiv e.org/details/bitsavers_ti dataBookVol2_4594535 2/page/n715)
74x171	4	quad D flip-flops, clear		16	SN74LS171 (https://arch ive.org/details/bitsavers _tidataBookVol2_459453 52/page/n725)
74x172	1	16-bit multiple port register file (8x2)	three- state	24	SN74172 (https://archiv e.org/details/bitsavers_ti dataBookVol2_4594535 2/page/n729)
74x173	4	quad D flip-flop, asynchronous clear	three- state	16	SN74173 (http://www.ti.c om/lit/gpn/sn54ls173a)
74x174	6	hex D flip-flop, common asynchronous clear		16	SN74174 (http://www.ti.c om/lit/gpn/sn74s175)
74x175	4	quad D edge-triggered flip- flop, complementary outputs and asynchronous clear		16	SN74175 (http://www.ti.c om/lit/gpn/sn74s175)

74x176	1	presettable decade (bi- quinary) counter/latch		14	SN74176 (https://archiv e.org/details/bitsavers_ti dataBookVol2_4594535 2/page/n745)
74x177	1	presettable binary counter/latch		14	SN74177 (https://archiv e.org/details/bitsavers_ti dataBookVol2_4594535 2/page/n745)
74x178	1	4-bit parallel-access shift register		14	SN74178 (https://archiv e.org/details/bitsavers_ti dataBookVol2_4594535 2/page/n751)
74x179	1	4-bit parallel-access shift register, asynchronous clear input, complementary Q _d output		16	SN74179 (https://archiv e.org/details/bitsavers_ti dataBookVol2_4594535 2/page/n751)
74x180	1	9-bit odd/even <u>parity bit</u> generator and checker		14	SN74180 (https://archiv e.org/details/bitsavers_ti dataBookVol2_4594535 2/page/n755)
<u>74x181</u>	1	4-bit arithmetic logic unit and function generator		24	SN74LS181 (http://www. ti.com/lit/gpn/sn54ls181)
74x182	1	lookahead carry generator		16	SN74S182 (https://web. archive.org/web/2016041 8004301/http://www.ti.co m/lit/ds/symlink/sn74s1 82.pdf)
74x183	2	dual carry-save full adder		14	SN74LS183 (https://arch ive.org/details/bitsavers _tidataBookVol2_459453 52/page/n777)
74x184	1	BCD to binary converter	open- collector	16	SN74184 (https://archiv e.org/details/bitsavers_ti dataBookVol2_4594535 2/page/n781)
74x185	1	6-bit binary to BCD converter	open- collector	16	SN74185A (https://archi ve.org/details/bitsavers_ tidataBookVol2_4594535 2/page/n781)
74x186	1	512-bit <u>ROM</u> (64x8)	open- collector	24	SN74186 (https://archiv e.org/details/bitsavers_ti dataBookForDesignEngi neers2ed_29954976/pag e/n121)
74x187	1	1024-bit <u>ROM</u> (256x4)	open- collector	16	SN74187 (https://archiv e.org/details/bitsavers_ti dataBookcomputerComp onentsDataBook_16851 665/page/n181)
74x188	1	256-bit <u>PROM</u> (32x8)	open- collector	16	SN74S188 (https://archi ve.org/details/bitsavers_ tidataBookcomputerCom ponentsDataBook_1685 1665/page/n173)

74x189	1	64-bit RAM (16x4), 4 data inputs, 4 inverted data outputs		three- state	16	SN74S189 (https://archi ve.org/details/bitsavers_ tidataBookcomputerCom ponentsDataBook_1685 1665/page/n191)
74x190	1	synchronous presettable up/down 4-bit decade counter			16	SN74190 (http://www.ti.c om/lit/gpn/sn74ls191)
74x191	1	synchronous presettable up/down 4-bit binary counter			16	SN74191 (http://www.ti.c om/lit/gpn/sn74ls191)
74x192	1	synchronous presettable up/down 4-bit decade counter, clear			16	SN74192 (http://www.ti.c om/lit/gpn/sn74ls193)
74x193	1	synchronous presettable up/down 4-bit binary counter, clear			16	SN74193 (http://www.ti.c om/lit/gpn/sn74ls193)
74x194	1	4-bit bidirectional universal shift register			16	SN74194 (https://archiv e.org/details/bitsavers_ti dataBookVol2_4594535 2/page/n820)
74x195	1	4-bit parallel-access shift register			16	SN74195 (https://archiv e.org/details/bitsavers_ti dataBookVol2_4594535 2/page/n829)
74x196	1	presettable 4-bit decade counter/latch			14	SN74196 (https://archiv e.org/details/bitsavers_ti dataBookVol2_4594535 2/page/n837)
74x197	1	presettable 4-bit binary counter/latch			14	SN74197 (https://archiv e.org/details/bitsavers_ti dataBookVol2_4594535 2/page/n837)
74x198	1	8-bit bidirectional universal shift register			24	SN74198 (https://web.ar chive.org/web/20070228 042947/http://focus.ti.co m/lit/ds/symlink/sn7419 8.pdf)
74x199	1	8-bit universal shift register, J-NotK serial inputs			24	SN74199 (https://web.ar chive.org/web/20070228 042947/http://focus.ti.co m/lit/ds/symlink/sn7419 8.pdf)
Part number	Units	Description	Input	Output	Pins	Datasheet
74x200	1	256-bit RAM (256x1)		three- state	16	DM74S200 (https://archi ve.org/details/bitsavers_ nationaldaTTLDatabook_ 42712617/page/n299)
74x201	1	256-bit RAM (256x1)		three- state	16	SN74S201 (https://archi ve.org/details/bitsavers_ tidataBookcomputerCom ponentsDataBook_1685 1665/page/n195)
74x202	1	256-bit RAM (256x1) with power down		three- state	16	SN74LS202 (https://arch ive.org/details/bitsavers

					_tidataBook2ed05_2617 547/page/n51)
74x206	1	256-bit RAM (256x1)	open- collector	16	DM74S206 (https://archi ve.org/details/bitsavers_ nationaldaTTLDatabook_ 42712617/page/n301)
74x207	1	1024-bit RAM (256x4)	three- state	16	SN74LS207 (https://arch ive.org/details/bitsavers _tidataBookcomputerCo mponentsDataBook_168 51665/page/n205)
74x208	1	1024-bit RAM (256x4), separate data in- and outputs	three- state	20	SN74LS208 (https://arch ive.org/details/bitsavers _tidataBookcomputerCo mponentsDataBook_168 51665/page/n205)
74x209	1	1024-bit RAM (1024x1)	three- state	16	SN74S209 (https://archi ve.org/details/bitsavers_ tidataBookmoryDataBoo k1975_9924035/page/n1 71)
74x210	8	octal buffer, inverting	three- state	20	SN74LS210 (https://arch ive.org/stream/Monolithi cMemories-MMI-Bipolar LSI1982DatabookOCR# page/n311)
74x211	1	144-bit RAM (16x9) with output latch	three- state	20	74F211 (https://archive. org/details/bitsavers_fair childdldFASTDataBook_ 29981933/page/n181)
74x212	1	144-bit RAM (16x9)	three- state	20	74F212 (https://archive. org/details/bitsavers_fair childdldFASTDataBook_ 29981933/page/n185)
74x213	1	192-bit RAM (16x12)	three- state	20	74F213 (https://archive. org/details/bitsavers_fair childdldFASTDataBook_ 29981933/page/n189)
74x214	1	1024-bit RAM (1024x1)	three- state	16	SN74LS214 (https://arch ive.org/details/bitsavers _tidataBookcomputerCo mponentsDataBook_168 51665/page/n199)
74x215	1	1024-bit RAM (1024x1) with power-down mode	three- state	16	SN74LS215 (https://arch ive.org/details/bitsavers _tidataBookcomputerCo mponentsDataBook_168 51665/page/n199)
74x216	1	256-bit RAM (64x4), common I/O	three- state	16	SN74LS216 (https://data sheet.datasheetarchive. com/originals/distributor s/Datasheets-112/DSAP 0044696.pdf)
74x217	1	256-bit RAM (64x4)	three- state	20	SN74ALS217 (https://ar chive.org/details/bitsave rs_tidataBookuitsDataBo

							ok_32771470/page/n17 3)
	74x218	1	256-bit RAM (32x8)		three- state	20	SN74ALS218 (https://ar chive.org/details/bitsave rs_tidataBookuitsDataBo ok_32771470/page/n17 3)
	74x219	1	64-bit RAM (16x4), non- inverting outputs		three- state	16	SN74LS219 (https://arch ive.org/stream/Supplem entToTheTTLDataBookF orDesignEngineers2ndE dition/Supplement%20t o%20The%20TTL%20D ata%20Book%20for%20 Design%20Engineers_2 nd_Edition#page/n5)
	74x221	2	dual monostable multivibrator	Schmitt trigger		16	SN74221 (http://www.ti.c om/lit/gpn/sn74221)
	74x222	1	64-bit <u>FIFO</u> memory (16x4), synchronous, input/output ready enable		three- state	20	SN74LS222 (http://www. ralphselectronics.com/pr oductimages/SEMI-SN7 4LS224N.PDF)
	74x224	1	64-bit <u>FIFO</u> memory (16x4), synchronous		three- state	16	SN74LS224 (http://www. ralphselectronics.com/pr oductimages/SEMI-SN7 4LS224N.PDF)
	74x225	1	80-bit FIFO memory (16x5), asynchronous		three- state	20	SN74S225 (http://www.t i.com/lit/gpn/sn74s225)
	74x226	1	4-bit parallel latched bus transceiver		three- state	16	SN74S226 (https://archi ve.org/details/bitsavers_ tidataBookcomputerCom ponentsDataBook_1685 1665/page/n219)
	74x227	1	64-bit <u>FIFO</u> memory (16x4), synchronous, input/output ready enable		open- collector	20	SN74LS727 (http://www. ralphselectronics.com/pr oductimages/SEMI-SN7 4LS224N.PDF)
	74x228	1	64-bit <u>FIFO</u> memory (16x4), synchronous		open- collector	20	SN74LS728 (http://www. ralphselectronics.com/pr oductimages/SEMI-SN7 4LS224N.PDF)
	74x229	1	80-bit FIFO memory (16x5), asynchronous		three- state	20	SN74ALS229B (https:// web.archive.org/web/200 70101063514/http://focu s.ti.com/lit/ds/symlink/s n74als229b.pdf)
	74x230	2	dual 4-bit buffer/driver, one inverted, one non-inverted; negative enable		three- state	20	SN74AS230 (https://arc hive.org/details/bitsaver s_tidataBookVol3_25840 031/page/n245)
	74x231	2	dual 4-bit buffer/driver, both inverted; one positive and one negative enable		three- state	20	SN74AS231 (https://arc hive.org/details/bitsaver s_tidataBookVol3_25840 031/page/n245)
-	74x232	1	64-bit FIFO memory (16x4), asynchronous		three- state	16	SN74ALS232B (http://w ww.ti.com/lit/gpn/sn74al

						<u>s232b)</u>
74x233	1	80-bit FIFO memory (16x5), asynchronous		three- state	20	SN74ALS233B (https://a rchive.org/details/bitsav ers_tidataBookeFIFOMe moriesDatabook_633528 41/page/n101)
74x234	1	256-bit FIFO memory (64x4), asynchronous		three- state	16	SN74ALS234 (https://ar chive.org/details/bitsave rs_tidataBookeFIFOMe moriesDatabook_633528 41/page/n63)
74x235	1	320-bit FIFO memory (64x5), asynchronous		three- state	20	SN74ALS235 (https://ar chive.org/details/bitsave rs_tidataBookeFIFOMe moriesDatabook_633528 41/page/n109)
74x236	1	256-bit FIFO memory (64x4), asynchronous		three- state	16	SN74ALS236 (https://we b.archive.org/web/20070 102044700/http://focus.t i.com/lit/ds/symlink/sn7 4als236.pdf)
74x237	1	3-to-8 line decoder/demultiplexer, address latch, active high outputs			16	CD74HC237 (http://www. ti.com/lit/gpn/cd54hc23 7)
74x238	1	3-to-8 line decoder/demultiplexer, active high outputs			16	CD74HC238 (http://www. ti.com/lit/gpn/CD74HC23 8)
74x239	2	dual 2-to-4 line decoder/demultiplexer, active high outputs			16	SN74HC239 (https://arc hive.org/details/bitsaver s_tidataBookogicDataBo ok_23574286/page/n24 1)
74x240	8	octal buffer, inverting outputs	Schmitt trigger	three- state	20	SN74LS240 (http://www. ti.com/lit/gpn/sn54ls240)
74x241	8	octal buffer, non-inverting outputs	Schmitt trigger	three- state	20	SN74LS241 (http://www. ti.com/lit/gpn/sn54ls240)
74x242	4	quad bus transceiver, inverting outputs	Schmitt trigger	three- state	14	SN74LS242 (https://we b.archive.org/web/20040 608202058/http://focus.t i.com/lit/ds/symlink/sn7 4ls242.pdf)
74x243	4	quad bus transceiver, non- inverting outputs	Schmitt trigger	three- state	14	SN74LS243 (http://www. ti.com/lit/gpn/sn74ls243)
74x244	8	octal buffer, non-inverting outputs	Schmitt trigger	three- state	20	SN74LS244 (http://www. ti.com/lit/gpn/sn54ls240)
74x245	8	octal bus transceiver, non- inverting outputs	Schmitt trigger	three- state	20	SN74LS245 (http://www. ti.com/lit/gpn/sn74ls245)
74x246	1	BCD to 7-segment decoder/driver		open- collector 30 V	16	SN74246 (http://www.ti.c om/lit/gpn/sn74ls247)
74x247	1	BCD to 7-segment decoder/driver		open- collector 15 V	16	SN74247 (http://www.ti.c om/lit/gpn/sn74ls247)

74x248	1	BCD to 7-segment decoder/driver	open- collector, 2 kΩ pull-up	16	SN74248 (http://www.ti.c om/lit/gpn/sn74ls247)
74x249	1	BCD to 7-segment decoder/driver	open- collector	16	SN74249 (https://archiv e.org/details/bitsavers_ti dataBookVol2_4594535 2/page/n879)
74x250	1	1 of 16 data selector/multiplexer	three- state	24	SN74AS250 (https://arc hive.org/details/bitsaver s_tidataBookVol3_25840 031/page/n273)
74x251	1	8-line to 1-line data selector/multiplexer, complementary outputs	three- state	16	SN74251 (http://www.ti.c om/lit/gpn/sn74ls251)
74x253	2	dual 4-line to 1-line data selector/multiplexer	three- state	16	SN74LS253 (http://www. ti.com/lit/gpn/sn74ls253)
74x255	2	dual 2-to-4 line decoder/demultiplexer, inverting outputs	three- state	16	74LS255 (https://archiv e.org/details/bitsavers_i cMaster19_198675341/p age/n315)
74x256	2	dual 4-bit addressable latch		16	MC74F256 (https://archi ve.org/details/bitsavers_ motoroladaFASTandLST TLData_35934218/page/ n161)
74x257	4	quad 2-line to 1-line data selector/multiplexer, non- inverting outputs	three- state	16	SN74LS257B (http://ww w.ti.com/lit/gpn/sn74ls25 7b)
74x258	4	quad 2-line to 1-line data selector/multiplexer, inverting outputs	three- state	16	SN74LS258B (http://ww w.ti.com/lit/gpn/sn74ls25 7b)
74x259	1	8-bit bit addressable input latch with clr		16	SN74259 (http://www.ti.c om/lit/gpn/sn74ls259b)
74x260	2	dual 5-input NOR gate		14	SN74LS260 (http://pdf.d atasheetcatalog.com/dat asheets/90/488420_DS. pdf)
74x261	1	2-bit by 4-bit parallel binary multiplier		16	SN74LS261 (https://arch ive.org/details/bitsavers _tidataBookVol2_459453 52/page/n921)
74x262	1	5760-bit ROM (<u>Teletext</u> character set, 128 characters 5x9)	three- state	20	SN74S262N (https://dat asheet.datasheetarchiv e.com/originals/distribut ors/Datasheets-112/DSA P0044628.pdf)
74x264	1	look ahead carry generator		16	SN74AS264 (https://arc hive.org/details/bitsaver s_tidataBookVol3_25840 031/page/n295)
74x265	4	quad complementary output elements		16	SN74265 (https://archiv e.org/details/bitsavers_ti dataBookVol2_4594535 2/page/n927)

74x266	4	quad 2-input XNOR gate	open- collector	14	SN74LS266 (http://www. ti.com/lit/gpn/sn74ls266)
74x268	6	hex D-type latches, common output control, common enable	three- state	16	SN74S268 (https://archi ve.org/details/bitsavers_ tidataBookVol2_4594535 2/page/n935)
74x269	1	8-bit bidirectional binary counter		24	MC74F269 (https://archi ve.org/details/bitsavers_ motoroladaFASTandLST TLData_35934218/page/ n175)
74x270	1	2048-bit <u>ROM</u> (512x4)	open- collector	16	SN74S270 (https://archi ve.org/details/bitsavers_ tidataBookcomputerCom ponentsDataBook_1685 1665/page/n181)
74x271	1	2048-bit <u>ROM</u> (256x8)	open- collector	20	SN74S271 (https://archi ve.org/details/bitsavers_ tidataBookcomputerCom ponentsDataBook_1685 1665/page/n181)
74x273	1	8-bit register, asynchronous clear		20	SN74273 (http://www.ti.c om/lit/gpn/sn74ls273)
74x274	1	4-bit by 4-bit binary multiplier	three- state	20	SN74S274 (https://archi ve.org/details/bitsavers_ tidataBookForDesignEng ineers2ed_29954976/pag e/n647)
74x275	1	7-bit slice Wallace tree	three- state	16	SN74S275 (https://archi ve.org/details/bitsavers_ tidataBookForDesignEng ineers2ed_29954976/pag e/n647)
74x276	4	quad J-NotK edge-triggered flip-flops, separate clocks, common preset and clear		20	SN74276 (https://archiv e.org/details/bitsavers_ti dataBookVol2_4594535 2/page/n941)
74x278	1	4-bit cascadeable priority registers, latched data inputs		14	SN74278 (https://archiv e.org/details/bitsavers_ti dataBookVol2_4594535 2/page/n945)
74x279	4	quad set-reset latch		16	SN74279 (http://www.ti.c om/lit/gpn/sn54ls279a)
74x280	1	9-bit odd/even parity bit generator/checker		14	SN74LS280 (http://www. ti.com/lit/gpn/sn74ls280)
74x281	1	4-bit parallel binary accumulator		24	SN74S281 (https://archive.org/details/bitsavers_ tidataBookVol2_4594535 2/page/n959)
74x282	1	look-ahead carry generator, selectable carry inputs		20	SN74AS282 (https://arc hive.org/details/bitsaver s_tidataBookVol3_25840 031/page/n309)
74x283	1	4-bit binary <u>full adder</u> (has carry in function)		16	SN74283 (http://www.ti.c om/lit/gpn/sn74ls283)

74x284	1	4-bit by 4-bit parallel binary multiplier (high order 4 bits of product)			16	SN74284 (https://archiv e.org/details/bitsavers_ti dataBookVol2_4594535 2/page/n971)
74x285	1	4-bit by 4-bit parallel binary multiplier (low order 4 bits of product)			16	SN74285 (https://archiv e.org/details/bitsavers_ti dataBookVol2_4594535 2/page/n971)
74x286	1	9-bit parity generator/checker, bus driver parity I/O port			14	SN74AS286 (http://www. ti.com/lit/gpn/sn74as28 6)
74x287	1	1024-bit <u>PROM</u> (256x4)		three- state	16	SN74S287 (https://archi ve.org/details/bitsavers_ tidataBookcomputerCom ponentsDataBook_1685 1665/page/n173)
74x288	1	256-bit <u>PROM</u> (32x8)		three- state	16	SN74S288 (https://archi ve.org/details/bitsavers_ tidataBookcomputerCom ponentsDataBook_1685 1665/page/n173)
74x289	1	64-bit RAM (16x4), 4 data inputs, 4 inverted data outputs		open- collector	16	SN74S289 (https://archi ve.org/details/bitsavers_ tidataBookcomputerCom ponentsDataBook_1685 1665/page/n191)
74x290	1	decade counter (separate divide-by-2 and divide-by-5 sections)			14	SN74290 (http://www.ti.c om/lit/gpn/sn74ls293)
74x292	1	programmable frequency divider/digital timer			16	SN74LS292 (http://www. ti.com/lit/gpn/sn74ls292)
74x293	1	4-bit binary counter (separate divide-by-2 and divide-by-8 sections)			14	SN74293 (http://www.ti.c om/lit/gpn/sn74ls293)
74x294	1	programmable frequency divider/digital timer			16	SN74LS294 (http://www. ti.com/lit/gpn/sn74ls292)
74x295	1	4-bit bidirectional shift register		three- state	14	SN74LS295B (https://ar chive.org/details/bitsave rs_tidataBookVol2_4594 5352/page/n989)
74x297	1	digital phase-locked loop filter			16	SN74LS297 (http://www. ti.com/lit/gpn/sn74ls297)
74x298	4	quad 2-input multiplexer, storage			16	SN74298 (http://www.ti.c om/lit/gpn/sn74ls298)
74x299	1	8-bit bidirectional universal shift/storage register		three- state	20	SN74LS299 (http://www. ti.com/lit/gpn/sn74ls299)
Part number	Units	Description	Input	Output	Pins	Datasheet
74x300	1	256-bit <u>RAM</u> (256x1)		open- collector	16	SN74LS300A (https://arc hive.org/details/TexasIn struments-TI-Data-TheT TLDataBookforDesignEn gineersSecondEditionO CR/page/n135)

74x301	1	256-bit <u>RAM</u> (256x1)		open- collector	16	SN74S301 (https://archi ve.org/details/bitsavers_ tidataBookcomputerCom ponentsDataBook_1685 1665/page/n195)
74x302	1	256-bit RAM (256x1)		open- collector	16	SN74LS302 (https://arch ive.org/details/bitsavers _tidataBook2ed05_2617 547/page/n63)
74x303	1	octal divide-by-2 clock driver, 2 outputs inverted			16	SN74AS303 (https://arc hive.org/details/TexasIn struments-TI-Data-Adva ncedLogicandBusInterfa ceLogic1991OCR/page/n 515)
74x304	1	octal divide-by-2 clock driver			16	SN74AS304 (https://arc hive.org/details/TexasIn struments-TI-Data-Adva ncedLogicandBusInterfa ceLogic1991OCR/page/n 517)
74x305	1	octal divide-by-2 clock driver, 4 outputs inverted			16	SN74AS305 (https://arc hive.org/details/TexasIn struments-TI-Data-Adva ncedLogicandBusInterfa ceLogic1991OCR/page/n 521)
74x306	1	8-bit LV-TTL to <u>GTL+</u> bus transceiver		three- state and open- collector	(24)	SN74GTLPH306 (http s://www.ti.com/lit/gpn/S N74GTLPH306)
74x309	1	1024-bit RAM (1024x1)		open- collector	16	SN74S309 (https://archi ve.org/details/bitsavers_ tidataBookmoryDataBoo k1975_9924035/page/n1 71)
74x310	8	octal buffer, inverting	Schmitt trigger	three- state	20	SN74LS310 (https://arch ive.org/stream/Monolithi cMemories-MMI-Bipolar LSI1982DatabookOCR# page/n315)
74x311	1	144-bit RAM (16x9) with output latch		open- collector	20	74F311 (https://archive. org/details/bitsavers_fair childdldFASTDataBook_ 20099339/page/n303)
74x312	1	144-bit RAM (16x9)		open- collector	20	74F312 (https://archive. org/details/bitsavers_fair childdldFASTDataBook_ 20099339/page/n303)
74x313	1	192-bit RAM (16x12)		open- collector	20	74F313 (https://archive. org/details/bitsavers_fair childdldFASTDataBook_ 20099339/page/n303)
74x314	1	1024-bit RAM (1024x1)		open- collector	16	SN74LS314 (https://arch ive.org/details/bitsavers _tidataBookcomputerCo

						mponentsDataBook_168 51665/page/n199)
74x315	1	1024-bit RAM (1024x1) with power-down mode		open- collector	16	SN74LS315 (https://arch ive.org/details/bitsavers _tidataBookcomputerCo mponentsDataBook_168 51665/page/n199)
74x316	1	256-bit RAM (64x4), common I/O		open- collector	16	SN74LS316 (https://data sheet.datasheetarchive. com/originals/distributor s/Datasheets-112/DSAP 0044696.pdf)
74x317	1	256-bit RAM (64x4)		open- collector	20	SN74ALS317 (https://ar chive.org/details/bitsave rs_tidataBookuitsDataBo ok_32771470/page/n22 1)
74x318	1	256-bit RAM (32x8)		open- collector	20	SN74ALS318 (https://ar chive.org/details/bitsave rs_tidataBookuitsDataBo ok_32771470/page/n22 1)
74x319	1	64-bit <u>RAM</u> (16x4)		open- collector	16	SN74LS319 (https://arch ive.org/stream/Supplem entToTheTTLDataBookF orDesignEngineers2ndE dition/Supplement%20t o%20The%20TTL%20D ata%20Book%20for%20 Design%20Engineers_2 nd_Edition#page/n5)
74x320	1	crystal-controlled oscillator			16	SN74LS320 (https://arch ive.org/details/bitsavers _tidataBookVol2_459453 52/page/n1013)
74x321	1	crystal-controlled oscillators, F/2 and F/4 count-down outputs			16	SN74LS320 (https://arch ive.org/details/bitsavers _tidataBookVol2_459453 52/page/n1013)
74x322	1	8-bit shift register, sign extend		three- state	20	SN74LS322A (https://arc hive.org/details/bitsaver s_tidataBookVol2_45945 352/page/n1019)
74x323	1	8-bit bidirectional universal shift/storage register, synchronous clear		three- state	20	SN74LS323 (http://www. ti.com/lit/gpn/sn54ls323)
74x324	1	voltage-controlled oscillator (or crystal controlled), enable input, complementary outputs	analog		14	SN74LS324 (https://arch ive.org/details/bitsavers _tidataBook2ed07_2330 1973/page/n443)
74x325	2	dual voltage-controlled oscillator (or crystal controlled), complementary outputs	analog		16	SN74LS325 (https://arch ive.org/details/bitsavers _tidataBook2ed07_2330 1973/page/n443)
74x326	2	dual voltage-controlled oscillator (or crystal	analog		16	SN74LS326 (https://arch ive.org/details/bitsavers

		controlled), enable input, complementary outputs				_tidataBook2ed07_2330 1973/page/n443)
74x327	2	dual voltage-controlled oscillator (or crystal controlled)	analog		14	SN74LS327 (https://arch ive.org/details/bitsavers _tidataBook2ed07_2330 1973/page/n443)
74x330	1	PLA (12 inputs, 50 terms, 6 outputs)		three- state	20	SN74S330 (https://archi ve.org/details/bitsavers_ tidataBookcomputerCom ponentsDataBook_1685 1665/page/n231)
74x331	1	PLA (12 inputs, 50 terms, 6 outputs)		open- collector, 2.5 kΩ pull-up	20	SN74S331 (https://archi ve.org/details/bitsavers_ tidataBookcomputerCom ponentsDataBook_1685 1665/page/n231)
74x333	1	PLA (12 inputs, 32 terms, 6 outputs, 4 state registers)		three- state	24	SN74LS333 (https://data sheet.datasheetarchive. com/originals/distributor s/Datasheets-111/DSAP 0036733.pdf)
74x334	1	PLA (12 inputs, 32 terms, 6 outputs)		three- state	24	SN74LS334 (https://data sheet.datasheetarchive. com/originals/distributor s/Datasheets-111/DSAP 0036733.pdf)
74x335	1	PLA (12 inputs, 32 terms, 6 outputs, 4 state registers)		open- collector	24	SN74LS335 (https://data sheet.datasheetarchive. com/originals/distributor s/Datasheets-111/DSAP 0036733.pdf)
74x336	1	PLA (12 inputs, 32 terms, 6 outputs)		open- collector	24	SN74LS336 (https://data sheet.datasheetarchive. com/originals/distributor s/Datasheets-111/DSAP 0036733.pdf)
74x337	1	clock driver		three- state	20	SN74ABT337 (https://ar chive.org/details/Texasl nstruments-TI-Data-Adv ancedLogicandBusInterf aceLogic1991OCR/page/ n485)
74x340	8	octal buffer, inverting outputs	Schmitt trigger	three- state	20	SN74S340 (https://archi ve.org/details/bitsavers_ tidataBookForDesignEng ineers2ed_29954976/pag e/n701)
74x341	8	octal buffer, non-inverting outputs	Schmitt trigger	three- state	20	SN74S341 (https://archi ve.org/details/bitsavers_ tidataBookForDesignEng ineers2ed_29954976/pag e/n701)
74x344	8	octal buffer, non-inverting outputs	Schmitt trigger	three- state	20	SN74S344 (https://archi ve.org/details/bitsavers_ tidataBookForDesignEng ineers2ed_29954976/pag e/n701)

74x347	1	BCD to 7-segment decoders/drivers, low voltage version of 7447	open- collector	16	SN74LS347 (https://arch ive.org/details/bitsavers _tidataBookVol2_459453 52/page/n1027)
74x348	1	8 to 3-line priority encoder	three- state	16	SN74LS348 (http://www. ti.com/lit/gpn/sn74ls348)
74x350	1	4-bit shifter	three- state	16	SN74S350 (https://archi ve.org/details/bitsavers_ tidataBookVol2_4594535 2/page/n1035)
74x351	2	dual 8-line to 1-line data selectors/multiplexers, 4 common data inputs	three- state	20	SN74351 (https://archiv e.org/details/bitsavers_ti dataBookVol2_4594535 2/page/n1041)
74x352	2	dual 4-line to 1-line data selectors/multiplexers, inverting outputs		16	SN74LS352 (https://arch ive.org/details/bitsavers _tidataBookVol2_459453 52/page/n1045)
74x353	2	dual 4-line to 1-line data selectors/multiplexers, inverting outputs	three- state	16	SN74LS353 (https://arch ive.org/details/bitsavers _tidataBookVol2_459453 52/page/n1047)
74x354	1	8-line to 1-line data selector/multiplexer, transparent registers	three- state	20	CD74HC354 (http://www. ti.com/lit/gpn/cd54hc35 4)
74x355	1	8-line to 1-line data selector/multiplexer, transparent registers	open- collector	20	SN74LS355 (https://arch ive.org/details/bitsavers _tidataBookVol2_459453 52/page/n1051)
74x356	1	8-line to 1-line data selector/multiplexer, edge- triggered registers	three- state	20	CD74HCT356 (http://ww w.ti.com/lit/gpn/cd74hct3 56)
74x357	1	8-line to 1-line data selector/multiplexer, edge- triggered registers	open- collector	20	SN74LS357 (https://arch ive.org/details/bitsavers _tidataBookVol2_459453 52/page/n1051)
74x361	1	bubble memory function timing generator		22	SN74LS361 (https://data sheet.datasheetarchive. com/originals/distributor s/Datasheets-X2/DSA84 8000-290.pdf)
74x362	1	four-phase clock generator/driver for Texas Instruments TMS9900		20	SN74LS362 (https://arch ive.org/details/bitsavers _tidataBook2ed07_2330 1973/page/n457)
74x363	1	octal transparent latch	three- state	20	SN74LS363 (https://arch ive.org/details/bitsavers _tidataBook2ed07_2330 1973/page/n465)
74x364	1	octal edge-triggered D-type register	three- state	20	SN74LS364 (https://arch ive.org/details/bitsavers _tidataBook2ed07_2330 1973/page/n465)
74x365	6	hex buffer, non-inverting outputs	three- state	16	SN74LS365A (http://ww w.ti.com/lit/gpn/sn54ls36

					<u>6a)</u>
74x366	6	hex buffer, inverting outputs	three- state	16	SN74HC366 (http://www. ti.com/lit/ds/symlink/sn5 4hc366.pdf)
74x367	6	hex buffer, non-inverting outputs	three- state	16	SN74LS367A (http://ww w.ti.com/lit/gpn/sn54ls36 6a)
74x368	6	hex buffer, inverting outputs	three- state	16	SN74LS368A (http://ww w.ti.com/lit/gpn/sn54ls36 6a)
74x370	1	2048-bit <u>ROM</u> (512x4)	three- state	16	SN74S370 (https://archi ve.org/details/bitsavers_ tidataBookcomputerCom ponentsDataBook_1685 1665/page/n181)
74x371	1	2048-bit <u>ROM</u> (256x8)	three- state	20	SN74S371 (https://archi ve.org/details/bitsavers_ tidataBookcomputerCom ponentsDataBook_1685 1665/page/n181)
74x373	8	octal transparent latch	three- state	20	SN74LS373 (http://www. ti.com/lit/gpn/sn54ls373)
74x374	8	octal register	three- state	20	SN74LS374 (http://www. ti.com/lit/gpn/sn54ls373)
74x375	4	quad bistable latch		16	SN74LS375 (http://www. ti.com/lit/gpn/sn74ls375)
74x376	4	quad J-NotK flip-flop, common clock and common clear		16	SN74376 (https://archiv e.org/details/bitsavers_ti dataBookVol2_4594535 2/page/n1081)
74x377	1	8-bit register, clock enable		20	SN74LS377 (http://www. ti.com/lit/gpn/sn74ls377)
74x378	1	6-bit register, clock enable		16	SN74LS378 (http://www. ti.com/lit/gpn/sn74ls377)
74x379	1	4-bit register, clock enable and complementary outputs		16	SN74LS379 (http://www. ti.com/lit/gpn/sn74ls377)
74x380	1	8-bit multifunction register (combines features of x374, x377, x273, x534 ICs)	three- state	24	SN74LS380 (https://arch ive.org/stream/Monolithi cMemories-MMI-Bipolar LSI1982DatabookOCR# page/n193)
74x381	1	4-bit arithmetic logic unit/function generator, generate and propagate outputs		20	SN74LS381A (https://arc hive.org/details/bitsaver s_tidataBookVol2_45945 352/page/n1087)
74x382	1	4-bit arithmetic logic unit/function generator, ripple carry and overflow outputs		20	SN74LS382 (https://arch ive.org/details/bitsavers _tidataBookVol2_459453 52/page/n1087)
74x383	1	8-bit register	open- collector	20	SN74S383 (https://archi ve.org/stream/Monolithic Memories-MMI-BipolarL SI1984DatabookOCR#p age/n433)

74x384	1	8-bit by 1-bit two's complement multipliers			16	SN74LS384 (https://arch ive.org/details/bitsavers tidataBookVol2_459453 52/page/n1095)
74x385	4	quad serial adder/subtractor			20	SN74LS385 (https://arch ive.org/details/bitsavers _tidataBookVol2_459453 52/page/n1099)
74x386	4	quad 2-input <u>XOR gate</u>			14	SN74LS386 (http://pdf.d atasheetcatalog.com/dat asheet/motorola/SN74L S386N.pdf)
74x387	1	1024-bit <u>PROM</u> (256x4)		open- collector	16	SN74S387 (https://archi ve.org/details/bitsavers_ tidataBookcomputerCom ponentsDataBook_1685 1665/page/n173)
74x388	1	4-bit D-type register		three- state and standard	16	Am74S388 (https://data sheet.datasheetarchive. com/originals/scans/Sca ns-000/Scans-0017104.p df)
74x390	2	dual 4-bit decade counter, asynchronous clear			16	SN74LS390 (http://www. ti.com/lit/gpn/sn74ls390)
74x393	2	dual 4-bit binary counter, asynchronous clear			14	SN74LS393 (http://www. ti.com/lit/gpn/sn74ls390)
74x395	1	4-bit cascadable shift register		three- state	16	SN74LS395A (https://we b.archive.org/web/20070 101063359/http://focus.t i.com/lit/ds/symlink/sn7 4ls395a.pdf)
74x396	8	octal storage registers, parallel access			16	SN74LS396 (https://arch ive.org/details/bitsavers _tidataBookVol2_459453 52/page/n1119)
74x398	4	quad 2-input multiplexers, storage and complementary outputs			20	SN74LS398 (https://arch ive.org/details/bitsavers _tidataBookVol2_459453 52/page/n1119)
74x399	4	quad 2-input multiplexer, storage			16	SN74LS399 (http://www. ti.com/lit/gpn/sn74ls399)
Part number	Units	Description	Input	Output	Pins	Datasheet
74x401	1	CRC generator/checker			14	74F401 (https://archive. org/stream/NationalSemi conductor1988FASTAdv ancedSchottkyDataboo k/National%20Semicond uctor%201988%20FAS T%20Advanced%20Sch ottky%20Databook#pag e/n371)
74x402	1	serial data polynomial generator/checker			16	74F402 (https://archive. org/stream/NationalSemi conductor1988FASTAdv ancedSchottkyDataboo k/National%20Semicond

74x403164-bit FIFO memory (16x4)three-state2474F436 (true: //achive.sec) conductor/s201988ASTAGW conductor/s201988ASTAGW conductor/s201988ASTAGW conductor/s201988ASTAGW conductor/s201988ASTAGW conductor/s201988ASTAGW conductor/s201988ASTAGW conductor/s201988ASTAGW conductor/s201988ASTAGW conductor/s201988ASTAGW translation transceley2474F436 (true: //achive.com/data asheet/CEMI/mXy2tytt, d0)74x40513-to-8 line decoder (equivalent to Intel 8205)214UCY745206 (thr)://jrd1 disabsect/catalog.com/data asheet/CEMI/mXy2tytt, d0)744061ESD-protected voltage- translation transceiver(49)SN74AVCA406 (thr):://irc1 www.ti.com/datasSemi/Com/data com/datasSemi/Com/datasSemi/Com/data com/datasSemi/Com/databoSN74AVCA406 (thr):://irc1 www.ti.com/datasSemi/Com/databo krauced%205AST translation transceiver440SN74AVCA406 (thr):://irc1 www.ti.com/databo74x4071data access registerthree- state24MC74408 (thr):://irc1/ir www.ti.com/databo krauced%205AST trave204080/CASS trave204080/							uctor%201988%20FAS T%20Advanced%20Sch ottky%20Databook#pag e/n375)
74x40513-to-8 line decoder (equivalent to Intel 8205)16UCY74205 (http://acthi asheet/CEM/mXyztyxt. pdf)7440613-to-8 line decoder??14MC74406F (https://archi ve.org/details/Digital TC zeguvalents/page/n113)744061ESD-protected voltage- translation transceiver(48)SN74AVCA406 (https://archi ve.org/details/Digital TC zeguvalents/page/n113)74AvCA4061ESD-protected voltage- translation transceiver(48)SN74AVCA406 (https://archive. 	74x403	1	64-bit FIFO memory (16x4)		three- state	24	74F403 (https://archive. org/stream/NationalSemi conductor1988FASTAdv ancedSchottkyDataboo k/National%20Semicond uctor%201988%20FAS T%20Advanced%20Sch ottky%20Databook#pag e/n383)
7440613-to-8 line decoder??14MC74406P (https://archive.org/details/Digital IC Equivalents/page/n113)74AVCA4061ESD-protected voltage- translation transceiver(48)SN74AVCA406 (https:// Www.ti.com/lift/gpr/SN74 AVCA406)74x4071data access registerthree- state2474F407 (https://archive. org/stream/NationalSemi conductor1989FASTAAv arcedSchottkyDataboo k/MationalSemi ent/401374x4071data access registerthree- state24MC74408 (https://archive. org/stream/NationalSemi conductor1989FASTAAv arcedSchottkyDataboo k/MationalSemi ent/4013MC74408 (https://archive. org/stream/NationalSemi conductorDataLib erg/details/Disavers motoriadauctorDataLib motoriadauctorDataLib Memories-MMI-Bipolart. S11984DatabookOCCR#p age/n273)SN74S408 (https://archive. org/stream/Monolithic Memories-MMI-Bipolart. S11984DatabookOCCR#p 	74x405	1	3-to-8 line decoder (equivalent to Intel 8205)			16	UCY74S405 (http://pdf.d atasheetcatalog.com/dat asheet/CEMI/mXyztyxt. pdf)
74AVCA4061ESD-protected voltage- translation transceiver(48)SN74AVCA406 (https:// www.ti.com/lif.gpn/SN74 AVCA406)74x4071data access registerthree- state2474F407 (https://archive. org/stream/National/Semi conductor)988FASTA/v ancedSchotky/Databoo k/National%20Semicond wc/6201988/20FAS T%20Advanced%20SchMC74408 (https://archive. org/stream/National/Semi ancedSchotky/Databoo 	74406	1	3-to-8 line decoder	?	?	14	MC74406P (https://archi ve.org/details/Digital_IC _Equivalents/page/n113)
74x4071data access registerthree- state2474F407 (https://archive. org/stream/NationalSemi conductor1988FASTAdv arcedSchottkyDataboo k/National%20Dsemicond uctor%201988%20FAS7440818-bit parity tree14MC74408 (https://archive. 	74AVCA406	1	ESD-protected voltage- translation transceiver			(48)	SN74AVCA406 (https:// www.ti.com/lit/gpn/SN74 AVCA406)
7440818-bit parity tree14MC74408 (https://archiv e.org/details/bitsavers_motoroladauctorDataLibr aryVol8Chips_17508458/ page/n407)74S4081controller/driver for 16k/64k/256k dRAM48SN74S408 (https://archiv e.org/stream/Monolithic Memories-MMI-BipolarL SI1984DatabookOCR#p age/n273)74x4091controller/driver for 16k/64k/256k dRAM48SN74S409 (https://archi 	74x407	1	data access register		three- state	24	74F407 (https://archive. org/stream/NationalSemi conductor1988FASTAdv ancedSchottkyDataboo k/National%20Semicond uctor%201988%20FAS T%20Advanced%20Sch ottky%20Databook#pag e/n401)
74S4081controller/driver for 16k/64k/256k dRAM48SN74S408 (https://archi ve.org/stream/Monolithic Memories-MMI-BipolarL Si1984DatabookOCR#p age/n273)74x4091controller/driver for 16k/64k/256k dRAM48SN74S409 (https://archi ve.org/stream/Monolithic Memories-MMI-BipolarL Si1984DatabookOCR#p age/n273)74x409164-bit RAM (16x4) with output register48T4F410 (https://archive. org/stream/NationalSemi conductor1988FASTAdv ancedSchottkyDatabook (K/National%20Semicond uctor%201988%20FAS T%20Advanced%20Sch ottky%20Databook#pag e/n407)74x4111FIFO RAM controller40T4F411 (https://archive. org/details/bitsavers_fair	74408	1	8-bit parity tree			14	MC74408 (https://archiv e.org/details/bitsavers_ motoroladauctorDataLibr aryVol8Chips_17508458/ page/n407)
74x4091controller/driver for 16k/64k/256k dRAM48SN74S409 (https://archi ve.org/stream/Monolithic Memories-MMI-BipolarL S11984DatabookOCR#p age/n291)74x410164-bit RAM (16x4) with output registerthree- state1874F410 (https://archive. org/stream/NationalSemi conductor1988FASTAdv ancedSchottkyDataboo k/National%20Semicond uctor%201988%20FAS 	74S408	1	controller/driver for 16k/64k/256k dRAM			48	SN74S408 (https://archi ve.org/stream/Monolithic Memories-MMI-BipolarL SI1984DatabookOCR#p age/n273)
74x410164-bit RAM (16x4) with output registerthree- state1874F410 (https://archive. org/stream/NationalSemi conductor1988FASTAdv ancedSchottkyDataboo k/National%20Semicond uctor%201988%20FAS T%20Advanced%20Sch ottky%20Databook#pag e/n407)74x4111FIFO RAM controller4074F411 (https://archive. org/details/bitsavers_fair	74x409	1	controller/driver for 16k/64k/256k dRAM			48	SN74S409 (https://archi ve.org/stream/Monolithic Memories-MMI-BipolarL SI1984DatabookOCR#p age/n291)
74x411 1 FIFO RAM controller 40 74F411 (https://archive. org/details/bitsavers_fair	74x410	1	64-bit RAM (16x4) with output register		three- state	18	74F410 (https://archive. org/stream/NationalSemi conductor1988FASTAdv ancedSchottkyDataboo k/National%20Semicond uctor%201988%20FAS T%20Advanced%20Sch ottky%20Databook#pag e/n407)
	74x411	1	FIFO RAM controller			40	74F411 (https://archive. org/details/bitsavers_fair

					childdldFASTDataBook_ 29981933/page/n357)
74x412	1	multi-mode buffered 8-bit latches (equivalent to Intel 3212/8212)	three- state	24	SN74S412 (https://archi ve.org/details/bitsavers_ tidataBookcomputerCom ponentsDataBook_1685 1665/page/n247)
74x413	1	256-bit FIFO memory (64x4)		16	74F413 (https://archive. org/stream/NationalSemi conductor1988FASTAdv ancedSchottkyDataboo k/National%20Semicond uctor%201988%20FAS T%20Advanced%20Sch ottky%20Databook#pag e/n417)
74x414	1	interrupt priority controller for Intel 8080 (equivalent to Intel 8214)		24	UCY74S414 (http://pdf.d atasheetcatalog.com/dat asheet/CEMI/mXyztyxr. pdf)
74416	1	modulo 10 counter, preload and clear inputs		16	MC74416 ^{[8]:50}
74S416	1	4-bit bidirectional bus transceiver, non-inverting (equivalent to Intel 8216)	three- state	16	UCY74S416 (http://pdf.d atasheetcatalog.com/dat asheet/CEMI/mXyztyxq. pdf)
74x417	2	modulo 2 and modulo 5 counters, common preload and clear inputs		16	MC74417 (https://archiv e.org/details/bitsavers_ motoroladauctorDataLibr aryVol8Chips_17508458/ page/n409)
74418	1	modulo 16 counter, preload and clear inputs		16	MC74418 ^{[8]:51}
74F418	1	32-bit error detection and correction circuit	three- state	48	74F418 (https://archive. org/details/bitsavers_fair childdldFASTDataBook_ 29981933/page/n375)
74419	2	dual modulo 4 counters, common preload and clear inputs		16	MC74419 (https://archiv e.org/details/bitsavers_ motoroladauctorDataLibr aryVol8Chips_17508458/ page/n411)
74S419	1	FIFO RAM controller		40	74S419 (https://archive. org/details/bitsavers_m midataBook6ed_795792 13/page/n727)
74x420	1	32-bit check bit / syndrome bit generator	three- state	48	74F420 (https://archive. org/stream/NationalSemi conductor1988FASTAdv ancedSchottkyDataboo k/National%20Semicond uctor%201988%20FAS T%20Advanced%20Sch ottky%20Databook#pag e/n421)
74x422	1	retriggerable monostable multivibrators, two inputs		14	SN74LS422 (http://www. ti.com/lit/gpn/sn74ls423)

74x423	2	dual retriggerable monostable multivibrator		16	SN74LS423 (http://www. ti.com/lit/gpn/sn74ls423)
74424	2	dual voltage-controlled oscillator		14	MC74424 ^{[8]:52}
74LS424	1	two-phase clock generator/driver for Intel 8080 (equivalent to Intel 8224)		16	SN74LS424 (https://arch ive.org/details/bitsavers _tidataBook2ed07_2330 1973/page/n505)
74x425	4	quad bus buffers, active low enables	three- state	14	SN74425 (https://archiv e.org/details/bitsavers_ti dataBookVol2_4594535 2/page/n1139)
74x426	4	quad bus buffers, active high enables	three- state	14	SN74426 (https://archiv e.org/details/bitsavers_ti dataBookVol2_4594535 2/page/n1139)
74x428	1	system controller for Intel 8080A (equivalent to Intel 8228)		28	SN74S428 (https://archi ve.org/details/bitsavers_ tidataBookcomputerCom ponentsDataBook_1685 1665/page/n253)
74x429	1	FIFO RAM controller	three- state	28	74LS429 (https://datash eet.datasheetarchive.co m/originals/distributors/D atasheets-111/DSAP003 7196.pdf)
74x430	1	cyclic redundancy checker/corrector		28	74F430 (https://archive. org/details/bitsavers_fair childdldFASTDataBook_ 20099339/page/n309)
74x432	1	8-bit multi-mode buffered latch	three- state	24	74F432 (https://archive. org/stream/NationalSemi conductor1988FASTAdv ancedSchottkyDataboo k/National%20Semicond uctor%201988%20FAS T%20Advanced%20Sch ottky%20Databook#pag e/n425)
74x433	1	256-bit FIFO memory (64x4)	three- state	24	74F433 (https://archive. org/stream/NationalSemi conductor1988FASTAdv ancedSchottkyDataboo k/National%20Semicond uctor%201988%20FAS T%20Advanced%20Sch ottky%20Databook#pag e/n431)
74x436	1	line driver/memory driver circuits - MOS memory interface, damping output resistor		16	SN74S436 (https://archive.org/details/bitsavers_ tidataBookVol2_4594535 2/page/n1143)
74x437	1	line driver/memory driver circuits - MOS memory interface		16	SN74S437 (https://archi ve.org/details/bitsavers_ tidataBookVol2_4594535 2/page/n1143)

74x438	1	system controller for Intel 8080A (equivalent to Intel 8238)			28	SN74S438 (https://archi ve.org/details/bitsavers_ tidataBookcomputerCom ponentsDataBook_1685 1665/page/n253)
74x440	4	quad tridirectional bus transceiver, non-inverting outputs		open- collector	20	SN74LS440 (https://we b.archive.org/web/20070 102044619/http://focus.t i.com/lit/ds/symlink/sn7 4ls442.pdf)
74x441	4	quad tridirectional bus transceiver, inverting outputs		open- collector	20	SN74LS441 (https://we b.archive.org/web/20070 102044619/http://focus.t i.com/lit/ds/symlink/sn7 4ls442.pdf)
74x442	4	quad tridirectional bus transceiver, non-inverting outputs		three- state	20	SN74LS442 (https://we b.archive.org/web/20070 102044619/http://focus.t i.com/lit/ds/symlink/sn7 4ls442.pdf)
74x443	4	quad tridirectional bus transceiver, inverting outputs		three- state	20	SN74LS443 (https://arch ive.org/details/bitsavers _tidataBookVol2_459453 52/page/n1147)
74x444	4	quad tridirectional bus transceiver, inverting and non-inverting outputs		three- state	20	SN74LS444 (https://we b.archive.org/web/20070 102044619/http://focus.t i.com/lit/ds/symlink/sn7 4ls442.pdf)
74x445	1	BCD to decimal decoders/drivers		driver 80 mA	16	SN74LS445 (https://arch ive.org/details/bitsavers tidataBookVol2_459453 52/page/n1153)
74x446	4	quad bus transceivers, direction controls, inverting outputs		three- state	16	SN74LS446 (https://arch ive.org/details/bitsavers _tidataBookVol2_459453 52/page/n1155)
74x447	1	BCD to 7-segment decoders/drivers, low voltage version of 74247		open- collector	16	SN74LS447 (https://arch ive.org/details/bitsavers _tidataBookVol2_459453 52/page/n1159)
74x448	4	quad tridirectional bus transceiver, inverting and non-inverting outputs		open- collector	20	SN74LS448 (https://arch ive.org/details/bitsavers _tidataBookVol2_459453 52/page/n1147)
74x449	4	quad bus transceivers, direction controls, non- inverting outputs		three- state	16	SN74LS449 (https://arch ive.org/details/bitsavers _tidataBookVol2_459453 52/page/n1155)
74450	1	counter, latch, 7-segment decoder	?	open- collector	16	MC74450 (https://archiv e.org/details/bitsavers_ motoroladauctorDataLibr aryVol8Chips_17508458/ page/n419)
74S450	1	8192-bit PROM (1024x8) with power-down		three- state	24	SN74S450 (https://archi ve.org/details/bitsavers_ tidataBookcomputerCom

						ponentsDataBook_1685 1665/page/n177)
74LS450	1	16-to-1 multiplexer, complementary outputs			24	SN74LS450 (https://arch ive.org/stream/Monolithi cMemories-MMI-Bipolar LSI1982DatabookOCR# page/n201)
74S451	1	8192-bit PROM (1024x8) with power-down		open- collector	24	SN74S451 (https://archi ve.org/details/bitsavers_ tidataBookcomputerCom ponentsDataBook_1685 1665/page/n177)
74LS451	2	dual 8-to-1 multiplexer			24	SN74LS451 (https://arch ive.org/stream/Monolithi cMemories-MMI-Bipolar LSI1982DatabookOCR# page/n205)
74x452	2	dual decade counter, synchronous	?	?	16	MC74452 (https://archiv e.org/details/bitsavers_ motoroladauctorDataLibr aryVol8Chips_17508458/ page/n419)
74453	2	dual binary counter, synchronous	?	?	16	MC74453 (https://archiv e.org/details/bitsavers_ motoroladauctorDataLibr aryVol8Chips_17508458/ page/n421)
74LS453	4	quad 4-to-1 multiplexer			24	SN74LS453 (https://arch ive.org/stream/Monolithi cMemories-MMI-Bipolar LSI1982DatabookOCR# page/n209)
74x454	2	dual decade up/down counter, synchronous, preset input	?	?	24	MC74454 (https://archiv e.org/details/bitsavers_ motoroladauctorDataLibr aryVol8Chips_17508458/ page/n421)
74455	2	dual binary up/down counter, synchronous, preset input	?	?	24	MC74455 (https://archiv e.org/details/bitsavers_ motoroladauctorDataLibr aryVol8Chips_17508458/ page/n421)
74F455	1	octal buffer / line driver with parity, inverting		three- state	24	74F455 (https://archive. org/details/bitsavers_sig neticsdaManual_579666 40/page/n505)
74456	1	4-bit NBCD full adder	?	?	16	MC74456 (https://archiv e.org/details/bitsavers_ motoroladauctorDataLibr aryVol8Chips_17508458/ page/n421)
74F456	1	octal buffer / line driver with parity, non-inverting		three- state	24	74F456 (https://archive. org/details/bitsavers_sig neticsdaManual_579666 40/page/n505)
74x458	1	nines complement / zero element	?	?	14	MC74458 (https://archiv e.org/details/bitsavers_

						motoroladauctorDataLibr aryVol8Chips_17508458/ page/n423)
74460	1	4-bit bus transfer switch	?	three- state	16	MC74460 (https://archiv e.org/details/bitsavers_ motoroladauctorDataLibr aryVol8Chips_17508458/ page/n423)
74LS460	1	10-bit comparator			24	SN74LS460 (https://arch ive.org/stream/Monolithi cMemories-MMI-Bipolar LSI1984DatabookOCR# page/n219)
74x461	1	8-bit presettable binary counter		three- state	24	SN74LS461 (https://arch ive.org/stream/Monolithi cMemories-MMI-Bipolar LSI1982DatabookOCR# page/n185)
74x462	1	fiber-optic data-link transmitter		open- collector 100 mA and standard	20	SN74LS462 (https://data sheet.datasheetarchive. com/originals/scans/Sca ns-067/DSA2IH0021510 8.pdf)
74x463	1	fiber-optic data-link receiver	analog		20	SN74LS463 (https://data sheet.datasheetarchive. com/originals/scans/Sca ns-067/DSA2IH0021510 8.pdf)
74x465	8	octal buffer, non-inverting outputs		three- state	20	SN74LS465 (https://we b.archive.org/web/20070 101063029/http://focus.t i.com/lit/ds/symlink/sn7 4ls465.pdf)
74x466	8	octal buffers, inverting outputs		three- state	20	SN74LS466 (https://we b.archive.org/web/20070 101063029/http://focus.t i.com/lit/ds/symlink/sn7 4ls465.pdf)
74x467	8	octal buffers, non-inverting outputs		three- state	20	SN74LS467 (https://we b.archive.org/web/20070 101063029/http://focus.t i.com/lit/ds/symlink/sn7 4ls465.pdf)
74x468	8	octal buffers, inverting outputs		three- state	20	SN74LS468 (https://we b.archive.org/web/20070 101063029/http://focus.t i.com/lit/ds/symlink/sn7 4ls465.pdf)
74x469	1	8-bit synchronous up/down counter, parallel load and hold capability		three- state	24	SN74LS469 (https://arch ive.org/stream/Monolithi cMemories-MMI-Bipolar LSI1984DatabookOCR# page/n191)
74x470	1	2048-bit PROM (256x8)		open- collector	20	SN74S470 (https://archi ve.org/details/bitsavers_ tidataBookcomputerCom
					ponentsDataBook_1685 1665/page/n173)	
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74x471	1	2048-bit <u>PROM</u> (256x8)	three- state	20	SN74S471 (https://archi ve.org/details/bitsavers_ tidataBookcomputerCom ponentsDataBook_1685 1665/page/n173)	
74x472	1	4096-bit <u>PROM</u> (512x8)	three- state	20	SN74S472 (https://archi ve.org/details/bitsavers_ tidataBookcomputerCom ponentsDataBook_1685 1665/page/n173)	
74x473	1	4096-bit <u>PROM</u> (512x8)	open- collector	20	SN74S473 (https://archi ve.org/details/bitsavers_ tidataBookcomputerCom ponentsDataBook_1685 1665/page/n173)	
74x474	1	4096-bit <u>PROM</u> (512x8)	three- state	24	SN74S474 (https://archi ve.org/details/bitsavers_ tidataBookcomputerCom ponentsDataBook_1685 1665/page/n173)	
74x475	1	4096-bit <u>PROM</u> (512x8)	open- collector	24	SN74S475 (https://archi ve.org/details/bitsavers_ tidataBookcomputerCom ponentsDataBook_1685 1665/page/n173)	
74x476	1	4096-bit <u>PROM</u> (1024x4)	three- state	18	SN74S476 (https://archi ve.org/details/bitsavers_ tidataBookcomputerCom ponentsDataBook_1685 1665/page/n177)	
74x477	1	4096-bit <u>PROM</u> (1024x4)	open- collector	18	SN74S477 (https://archi ve.org/details/bitsavers_ tidataBookcomputerCom ponentsDataBook_1685 1665/page/n177)	
74x478	1	8192-bit <u>PROM</u> (1024x8)	three- state	24	SN74S478 (https://archi ve.org/details/bitsavers_ tidataBookcomputerCom ponentsDataBook_1685 1665/page/n177)	
74x479	1	8192-bit <u>PROM</u> (1024x8)	open- collector	24	SN74S479 (https://archi ve.org/details/bitsavers_ tidataBookcomputerCom ponentsDataBook_1685 1665/page/n177)	
74x480	1	single burst error recovery circuit		24	SN74S480 (https://archi ve.org/details/bitsavers_ mmidataBook6ed_79579 213/page/n727)	
74x481	1	4-bit slice cascadable processor elements		(48)	SN74S481 (https://archi ve.org/details/bitsavers_ tidataBookcomputerCom ponentsDataBook_1685 1665/page/n15)	

74x482	1	4-bit <u>slice</u> expandable control elements			20	SN74S482 (https://archi ve.org/details/bitsavers_ tidataBookcomputerCom ponentsDataBook_1685 1665/page/n259)
74x484	1	BCD-to-binary converter		three- state	20	SN74S484A (https://arch ive.org/details/bitsavers _tidataBook1986_14886 851/page/n379)
74x485	1	binary-to-BCD converter		three- state	20	SN74S485A (https://arch ive.org/details/bitsavers _tidataBook1986_14886 851/page/n379)
74x488	1	IEEE-488 bus interface			48	74ACT488 (https://archi ve.org/details/bitsavers_ fairchilddldFACTLogicDa taBook_27153725/page/ n261)
74x490	2	dual decade counter			16	SN74490 (https://archiv e.org/details/bitsavers_ti dataBookVol2_4594535 2/page/n1167)
74x491	1	10-bit binary up/down counter, limited preset		three- state	24	SN74LS491 (https://arch ive.org/stream/Monolithi cMemories-MMI-Bipolar LSI1982DatabookOCR# page/n197)
						SN74LS498 (https://arch
74x498	1	8-bit bidirectional shift register, parallel inputs		three- state	24	cMemories-MMI-Bipolar LSI1982DatabookOCR# page/n189)
74x498 Part number	1 Units	8-bit bidirectional shift register, parallel inputs Description	Input	three- state Output	24 Pins	CMemories-MMI-Bipolar LSI1982DatabookOCR# page/n189) Datasheet
74x498 Part number 74x500	1 Units 1	8-bit bidirectional shift register, parallel inputs Description 6-bit flash analog-to-digital converter (ADC)	Input analog	three- state Output	24 Pins 24	CMemories-MMI-Bipolar LSI1982DatabookOCR# page/n189) Datasheet 74F500 (https://archive. org/details/bitsavers_fair childdldFASTDataBook_ 29981933/page/n409)
74x498 Part number 74x500 74x502	1 Units 1	8-bit bidirectional shift register, parallel inputs Description 6-bit flash analog-to-digital converter (ADC) 8-bit successive approximation register	Input analog	three- state Output	24 Pins 24 16	CMemories-MMI-Bipolar LSI1982DatabookOCR# page/n189) Datasheet 74F500 (https://archive. org/details/bitsavers_fair childdldFASTDataBook_ 29981933/page/n409) 74LS502 (https://archiv e.org/details/bitsavers_f airchilddldTTLDataBook _39509923/page/n497)
74x498 Part number 74x500 74x502 74x503	1 Units 1 1	 8-bit bidirectional shift register, parallel inputs Description 6-bit flash analog-to-digital converter (ADC) 8-bit successive approximation register 8-bit successive approximation register with expansion control 	Input analog	three- state Output	24 Pins 24 16 16	CMemories-MMI-Bipolar LSI1982DatabookOCR# page/n189) Datasheet 74F500 (https://archive. org/details/bitsavers_fair childdldFASTDataBook_ 29981933/page/n409) 74LS502 (https://archiv e.org/details/bitsavers_f airchilddldTTLDataBook _39509923/page/n497) 74LS503 (https://archiv e.org/details/bitsavers_f airchilddldTTLDataBook _39509923/page/n501)
74x498 Part number 74x500 74x502 74x503 74x504	1 Units 1 1 1	 8-bit bidirectional shift register, parallel inputs Description 6-bit flash analog-to-digital converter (ADC) 8-bit successive approximation register 8-bit successive approximation register with expansion control 12-bit successive approximation register with expansion control 	Input	three- state Output	24 Pins 24 16 16 24	CMemories-MMI-Bipolar LSI1982DatabookOCR# page/n189) Datasheet 74F500 (https://archive. org/details/bitsavers_fair childdldFASTDataBook_ 29981933/page/n409) 74LS502 (https://archiv e.org/details/bitsavers_f airchilddldTTLDataBook 39509923/page/n497) 74LS503 (https://archiv e.org/details/bitsavers_f airchilddldTTLDataBook 39509923/page/n501) 74LS504 (https://archiv e.org/details/bitsavers_f airchilddldTTLDataBook _39509923/page/n501) 74LS504 (https://archiv e.org/details/bitsavers_f airchilddldTTLDataBook _39509923/page/n501)
74x498 Part number 74x500 74x502 74x503 74x504 74x505	1 Units 1 1 1 1	 8-bit bidirectional shift register, parallel inputs Description 6-bit flash analog-to-digital converter (ADC) 8-bit successive approximation register 8-bit successive approximation register with expansion control 12-bit successive approximation register with expansion control 8-bit successive approximation register with expansion control 8-bit successive approximation register with 8-bit successive approximation ADC 	Input analog analog	three- state Output	24 Pins 24 16 16 24 24 24	CMemories-MMI-Bipolar LSI1982DatabookOCR# page/n189) Datasheet 74F500 (https://archive. org/details/bitsavers_fair childdldFASTDataBook_ 29981933/page/n409) 74LS502 (https://archiv e.org/details/bitsavers_f airchilddldTTLDataBook _39509923/page/n497) 74LS503 (https://archiv e.org/details/bitsavers_f airchilddldTTLDataBook _39509923/page/n501) 74LS504 (https://archiv e.org/details/bitsavers_f airchilddldTTLDataBook _39509923/page/n501) 74LS504 (https://archiv e.org/details/bitsavers_f airchilddldTTLDataBook _39509923/page/n505) 74F505 (https://archive. org/details/bitsavers_fair childdldFASTDataBook_ _39509923/page/n505)

						SI1982DatabookOCR#p age/n289)
74x515	1	programmable mapping decoder (2-to-4 line decoder with 9 programmable enable inputs)			20	74HCT515 ^{[9]:310}
74x516	1	16-bit multiplier/divider			24	SN74S516 (https://archi ve.org/stream/Monolithic Memories-MMI-BipolarL SI1984DatabookOCR#p age/n365)
74x518	1	8-bit comparator	20 kΩ pull-up	open- collector	20	SN74ALS518 (http://ww w.ti.com/lit/gpn/sn54als5 20)
74x519	1	8-bit comparator		open- collector	20	SN74ALS519 (https://ar chive.org/details/bitsave rs_tidataBookVol3_2584 0031/page/n365)
74x520	1	8-bit comparator, inverting output	20 kΩ pull-up		20	SN74ALS520 (http://ww w.ti.com/lit/gpn/sn54als5 20)
74x521	1	8-bit comparator, inverting output			20	SN74ALS521 (http://ww w.ti.com/lit/gpn/sn54als5 20)
74x522	1	8-bit comparator, inverting output	20 kΩ pull-up	open- collector	20	SN74ALS522 (https://ar chive.org/details/bitsave rs_tidataBookVol3_2584 0031/page/n365)
74x524	1	8-bit registered comparator		open- collector	20	74F524 (https://archive. org/stream/NationalSemi conductor1988FASTAdv ancedSchottkyDataboo k/National%20Semicond uctor%201988%20FAS T%20Advanced%20Sch ottky%20Databook#pag e/n449)
74x525	1	16-bit programmable counter			28	74F525 (https://archive. org/stream/NationalSemi conductor1988FASTAdv ancedSchottkyDataboo k/National%20Semicond uctor%201988%20FAS T%20Advanced%20Sch ottky%20Databook#pag e/n457)
74x526	1	fuse programmable identity comparator, 16-bit			20	SN74ALS526 (https://ar chive.org/details/bitsave rs_tidataBookVol3_2584 0031/page/n371)
74x527	1	fuse programmable identity comparator, 8-bit + 4-bit conventional Identity comparator			20	SN74ALS527 (https://ar chive.org/details/bitsave rs_tidataBookVol3_2584 0031/page/n371)
74x528	1	fuse programmable Identity comparator, 12-bit			16	SN74ALS528 (https://ar chive.org/details/bitsave

						rs_tidataBookVol3_2584 0031/page/n371)
74x531	8	octal transparent latch		three- state	20	SN74S531 (https://archi ve.org/stream/Monolithic Memories-MMI-BipolarL SI1982DatabookOCR#p age/n329)
74x532	8	octal register		three- state	20	SN74S532 (https://archi ve.org/stream/Monolithic Memories-MMI-BipolarL SI1982DatabookOCR#p age/n329)
74x533	1	octal transparent latch, inverting outputs		three- state	20	CD74HC533 (http://www. ti.com/lit/gpn/cd74hct56 3)
74x534	1	octal register, inverting outputs		three- state	20	CD74HC534 (http://www. ti.com/lit/gpn/cd74hc56 4)
74x535	1	octal transparent latch, inverting outputs		three- state	20	SN74S535 (https://archi ve.org/stream/Monolithic Memories-MMI-BipolarL SI1982DatabookOCR#p age/n331)
74x536	1	octal register, inverting outputs		three- state	20	SN74S536 (https://archi ve.org/stream/Monolithic Memories-MMI-BipolarL SI1982DatabookOCR#p age/n331)
74x537	1	BCD to decimal decoder		three- state	20	MC74F537 (https://archi ve.org/details/bitsavers_ motoroladaFASTandLST TLData_35934218/page/ n247)
74x538	1	3-to-8 line decoder/demultiplexer		three- state	20	SN74ALS538 (https://ar chive.org/details/bitsave rs_tidataBookVol3_2584 0031/page/n389)
74x539	2	dual 2-to-4 line decoder/demultiplexer		three- state	20	SN74ALS539 (https://ar chive.org/details/bitsave rs_tidataBookVol3_2584 0031/page/n393)
74x540	1	octal buffer, inverting outputs	Schmitt trigger	three- state	20	SN74LS540 (http://www. ti.com/lit/gpn/sn54ls540)
74x541	1	octal buffer, non-inverting outputs	Schmitt trigger	three- state	20	SN74LS541 (http://www. ti.com/lit/gpn/sn54ls540)
74x543	1	octal registered transceiver, non-inverting		three- state	24	SN74F543 (http://www.ti. com/lit/gpn/sn74f543)
74x544	1	octal registered transceiver, inverting		three- state	24	MC74F544 (https://archi ve.org/details/bitsavers_ motoroladaFASTandLST TLData_35934218/page/ n261)
74x545	1	octal bidirectional transceiver, non-inverting		three- state	20	74F545 (https://archive. org/stream/NationalSemi conductor1988FASTAdv ancedSchottkyDataboo

					k/National%20Semicond uctor%201988%20FAS T%20Advanced%20Sch ottky%20Databook#pag e/n497)
74x546	1	8-bit bidirectional registered transceiver, non-inverting	thre sta	ee- te 24	SN74LS546 (https://arch ive.org/details/bitsavers _mmidataBook6ed_7957 9213/page/n589)
74LS547	1	8-bit bidirectional latched transceiver, non-inverting	thre sta	ee- te 24	SN74LS547 (https://arch ive.org/details/bitsavers _mmidataBook6ed_7957 9213/page/n589)
74F547	1	3-to-8 line decoder/demultiplexer with address latches and acknowledge output		20	74F547 (https://archive. org/stream/NationalSemi conductor1988FASTAdv ancedSchottkyDataboo k/National%20Semicond uctor%201988%20FAS T%20Advanced%20Sch ottky%20Databook#pag e/n501)
74LS548	1	8-bit two-stage pipelined register	thre sta	ee- te 24	SN74LS548 (https://arch ive.org/details/bitsavers _mmidataBook6ed_7957 9213/page/n637)
74F548	1	3-to-8 line decoder/demultiplexer with acknowledge output		20	74F548 (https://archive. org/stream/NationalSemi conductor1988FASTAdv ancedSchottkyDataboo k/National%20Semicond uctor%201988%20FAS T%20Advanced%20Sch ottky%20Databook#pag e/n505)
74x549	1	8-bit two-stage pipelined latch	thre sta	ee- te 24	SN74LS549 (https://arch ive.org/details/bitsavers _mmidataBook6ed_7957 9213/page/n637)
74x550	1	octal registered transceiver with status flags, non- inverting	thre sta	ee- te 28	74F550 (https://archive. org/stream/NationalSemi conductor1988FASTAdv ancedSchottkyDataboo k/National%20Semicond uctor%201988%20FAS T%20Advanced%20Sch ottky%20Databook#pag e/n509)
74x551	1	octal registered transceiver with status flags, inverting	thre sta	ee- 28 te 28	74F551 (https://archive. org/stream/NationalSemi conductor1988FASTAdv ancedSchottkyDataboo k/National%20Semicond uctor%201988%20FAS T%20Advanced%20Sch ottky%20Databook#pag e/n509)
74x552	1	octal registered transceiver with parity and flags	thre sta	ee- 28 te	74F552 (https://archive. org/stream/NationalSemi

					conductor1988FASTAdv ancedSchottkyDataboo k/National%20Semicond uctor%201988%20FAS T%20Advanced%20Sch ottky%20Databook#pag e/n515)
74x556	1	16x16-bit multiplier slice	three- state	(84)	74S556 (https://archive. org/details/bitsavers_m midataBook7ed_126879 625/page/n567)
74x557	1	8-bit by 8-bit multiplier	three- state	40	SN74S557 (https://archive.org/stream/Monolithic Memories-MMI-BipolarL SI1984DatabookOCR#p age/n381)
74x558	1	8-bit by 8-bit multiplier	three- state	40	SN74S558 (https://archive.org/stream/Monolithic Memories-MMI-BipolarL SI1984DatabookOCR#p age/n381)
74x559	1	8-bit expandable two's complement multiplier/divider	three- state	24	74F559 (https://archive. org/details/bitsavers_fair childdldFASTDataBook_ 20099339/page/n311)
74x560	1	4-bit decade counter	three- state	20	SN74ALS560A (https://a rchive.org/details/bitsav ers_tidataBookVol3_258 40031/page/n401)
74x561	1	4-bit binary counter	three- state	20	SN74ALS561A (https://w eb.archive.org/web/2017 0305192612/http://www.t i.com/lit/ds/symlink/sn7 4als561a.pdf)
74x563	1	8-bit D-type transparent latch, inverting outputs	three- state	20	SN74ALS563B (http://w ww.ti.com/lit/gpn/sn54al s563b)
74x564	1	8-bit D-type edge-triggered register, inverting outputs	three- state	20	SN74ALS564B (http://w ww.ti.com/lit/gpn/sn54al s564b)
74x566	1	8-bit bidirectional registered transceiver, inverting	three- state	24	SN74LS566 (https://arch ive.org/details/bitsavers _mmidataBook6ed_7957 9213/page/n589)
74x567	1	8-bit bidirectional latched transceiver, inverting	three- state	24	SN74LS567 (https://arch ive.org/details/bitsavers _mmidataBook6ed_7957 9213/page/n589)
74x568	1	decade up/down counter	three- state	20	SN74ALS568A (http://w ww.ti.com/lit/gpn/sn74al s569a)
74x569	1	binary up/down counter	three- state	20	SN74ALS569A (http://w ww.ti.com/lit/gpn/sn74al s569a)
74x570	1	2048-bit PROM (512x4)	open- collector	16	DM74S570 (https://archi ve.org/details/bitsavers_

					nationaldataBook_16727 669/page/n315)
74x571	1	2048-bit PROM (512x4)	three- state	16	DM74S571 (https://archive.org/details/bitsavers_ nationaldataBook_16727 669/page/n315)
74x572	1	4096-bit PROM (1024x4)	open- collector	18	DM74S572 (https://archi ve.org/details/bitsavers_ nationaldataBook_16727 669/page/n317)
74x573	1	octal D-type transparent latch	three- state	20	SN74ALS573C (http://w ww.ti.com/lit/gpn/sn74al s573c)
74x574	1	octal D-type edge-triggered flip-flop	three- state	20	SN74HC574 (http://www. ti.com/lit/ds/symlink/sn7 4hc574.pdf)
74x575	1	octal D-type edge-triggered flip-flop, synchronous clear	three- state	24	SN74ALS575A (http://w ww.ti.com/lit/gpn/sn74al s575a)
74x576	1	octal D-type edge-triggered flip-flop, inverting outputs	three- state	20	SN74ALS576B (http://w ww.ti.com/lit/gpn/sn74as 576)
74x577	1	octal D-type edge-triggered flip-flop, synchronous clear, inverting outputs	three- state	24	SN74ALS577A (http://w ww.ti.com/lit/gpn/sn74as 576)
74x579	1	8-bit bidirectional binary counter	three- state	20	MC74F579 (https://archi ve.org/details/bitsavers_ motoroladaFASTandLST TLData_35934218/page/ n273)
74x580	1	octal D-type transparent latch, inverting outputs	three- state	20	SN74ALS580B (http://w ww.ti.com/lit/gpn/sn74al s580b)
74x582	1	4-bit BCD arithmetic logic unit		24	74F582 (https://archive. org/stream/NationalSemi conductor1988FASTAdv ancedSchottkyDataboo k/National%20Semicond uctor%201988%20FAS T%20Advanced%20Sch ottky%20Databook#pag e/n551)
74x583	1	4-bit BCD adder		16	74F583 (https://archive. org/stream/NationalSemi conductor1988FASTAdv ancedSchottkyDataboo k/National%20Semicond uctor%201988%20FAS T%20Advanced%20Sch ottky%20Databook#pag e/n555)
74x588	1	octal bidirectional transceiver with IEEE-488 termination resistors	three- state	20	74F588 (https://archive. org/stream/NationalSemi conductor1988FASTAdv ancedSchottkyDataboo k/National%20Semicond uctor%201988%20FAS

						T%20Advanced%20Sch ottky%20Databook#pag e/n559)
74x589	1	8-bit shift register, input latch		three- state	16	SN74LS589 (https://arch ive.org/details/bitsavers _tidataBookVol2_459453 52/page/n1181)
74x590	1	8-bit binary counter, output registers		three- state	16	SN74LS590 (http://www. ti.com/lit/gpn/sn74ls590)
74x591	1	8-bit binary counter, output registers		open- collector	16	SN74LS591 (http://www. ti.com/lit/gpn/sn74ls590)
74x592	1	8-bit binary counter, input registers			16	SN74LS592 (http://www. ti.com/lit/gpn/sn74ls592)
74x593	1	8-bit binary counter, input registers		three- state	20	SN74LS593 (http://www. ti.com/lit/gpn/sn74ls592)
74x594	1	8-bit shift registers, serial-in, parallel-out, output latches		buffered	16	SN74LS594 (http://www. ti.com/lit/gpn/sn74ls594)
74x595	1	8-bit shift registers, serial-in, parallel-out, output latches, output enable		three- state	16	SN74LS595 (http://www. ti.com/lit/gpn/sn74ls595)
74x596	1	8-bit shift registers, serial-in, parallel-out, output latches, output enable		open- collector	16	SN74LS596 (http://www. ti.com/lit/gpn/sn74ls595)
74x597	1	8-bit shift registers, parallel- in, serial-out, input latches			16	SN74LS597 (http://www. ti.com/lit/gpn/sn74ls597)
74,4500	1	8-bit shift register, selectable		three-	20	SN74LS598 (http://www.
(4X598	1 ×	parallel-in/out input latches		state	20	ti.com/lit/gpn/sn74ls597)
74x598	1	parallel-in/out input latches 8-bit shift registers, serial-in, parallel-out, output latches		state open- collector	16	ti.com/lit/gpn/sn74ls597) SN74LS599 (http://www. ti.com/lit/gpn/sn74ls594)
74x598 74x599 Part number	1 Units	parallel-in/out input latches 8-bit shift registers, serial-in, parallel-out, output latches Description	Input	state open- collector Output	16 Pins	ti.com/lit/gpn/sn74ls597) SN74LS599 (http://www. ti.com/lit/gpn/sn74ls594) Datasheet
74x598 74x599 Part number 74x600	1 Units	parallel-in/out input latches8-bit shift registers, serial-in, parallel-out, output latchesDescriptiondynamic memory refresh controller, transparent and burst modes, for 4K or 16K dRAM	Input	state open- collector Output three- state	20 16 Pins 20	ti.com/lit/gpn/sn74ls597) SN74LS599 (http://www. ti.com/lit/gpn/sn74ls594) Datasheet SN74LS600A (https://arc hive.org/details/bitsaver s_tidataBookVol2_45945 352/page/n1217)
74x598 74x599 Part number 74x600 74x601	1 Units 1	parallel-in/out input latches8-bit shift registers, serial-in, parallel-out, output latchesDescriptiondynamic memory refresh controller, transparent and burst modes, for 4K or 16K dRAMdynamic memory refresh controller, transparent and burst modes, for 64K dRAM	Input	state open- collector Output three- state three- state	20 16 Pins 20 20	ti.com/lit/gpn/sn74ls597) SN74LS599 (http://www. ti.com/lit/gpn/sn74ls594) Datasheet SN74LS600A (https://arc hive.org/details/bitsaver s_tidataBookVol2_45945 352/page/n1217) SN74LS601A (https://arc hive.org/details/bitsaver s_tidataBookVol2_45945 352/page/n1217)
74x598 74x599 Part number 74x600 74x601 74x602	1 Units 1 1	parallel-in/out input latches8-bit shift registers, serial-in, parallel-out, output latchesDescriptiondynamic memory refresh controller, transparent and burst modes, for 4K or 16K dRAMdynamic memory refresh controller, transparent and burst modes, for 64K dRAMdynamic memory refresh controller, transparent and burst modes, for 64K dRAMdynamic memory refresh controller, cycle steal and burst modes, for 4K or 16K dRAM	Input	state open- collector Output three- state three- state three- state	20 16 Pins 20 20 20	ti.com/lit/gpn/sn74ls597) SN74LS599 (http://www. ti.com/lit/gpn/sn74ls594) Datasheet SN74LS600A (https://arc hive.org/details/bitsaver s_tidataBookVol2_45945 352/page/n1217) SN74LS601A (https://arc hive.org/details/bitsaver s_tidataBookVol2_45945 352/page/n1217) SN74LS602A (https://arc hive.org/details/bitsaver s_tidataBookVol2_45945 352/page/n1217)
74x598 74x599 Part number 74x600 74x601 74x602 74x603	1 Units 1 1 1	parallel-in/out input latches8-bit shift registers, serial-in, parallel-out, output latchesDescriptiondynamic memory refresh controller, transparent and burst modes, for 4K or 16K dRAMdynamic memory refresh controller, transparent and burst modes, for 64K dRAMdynamic memory refresh controller, cycle steal and burst modes, for 4K or 16K dRAMdynamic memory refresh controller, cycle steal and burst modes, for 4K or 16K dRAMdynamic memory refresh controller, cycle steal and burst modes, for 64K dRAMdynamic memory refresh controller, cycle steal and burst modes, for 64K dRAM	Input	state open- collector Output three- state three- state three- state three- state	20 16 Pins 20 20 20 20	ti.com/lit/gpn/sn74ls597) SN74LS599 (http://www. ti.com/lit/gpn/sn74ls594) Datasheet SN74LS600A (https://arc hive.org/details/bitsaver s_tidataBookVol2_45945 352/page/n1217) SN74LS601A (https://arc hive.org/details/bitsaver s_tidataBookVol2_45945 352/page/n1217) SN74LS602A (https://arc hive.org/details/bitsaver s_tidataBookVol2_45945 352/page/n1217) SN74LS603A (https://arc hive.org/details/bitsaver s_tidataBookVol2_45945 352/page/n1217)
74x598 74x599 Part number 74x600 74x601 74x602 74x603 74x603	1 Units 1 1 1 1	parallel-in/out input latches8-bit shift registers, serial-in, parallel-out, output latchesDescriptiondynamic memory refresh controller, transparent and burst modes, for 4K or 16K dRAMdynamic memory refresh controller, transparent and burst modes, for 64K dRAMdynamic memory refresh controller, transparent and burst modes, for 64K dRAMdynamic memory refresh controller, cycle steal and burst modes, for 4K or 16K dRAMdynamic memory refresh controller, cycle steal and burst modes, for 64K dRAMdynamic memory refresh controller, cycle steal and burst modes, for 64K dRAMdynamic memory refresh controller, cycle steal and burst modes, for 64K dRAMdynamic memory refresh controller, cycle steal and burst modes, for 64K dRAMoctal 2-input multiplexer, latch, high-speed	Input	state open- collector Output three- state three- state three- state three- state three- state	16 Pins 20 21 220 23 24 25 26	ti.com/lit/gpn/sn74ls597) SN74LS599 (http://www. ti.com/lit/gpn/sn74ls594) Datasheet SN74LS600A (https://arc hive.org/details/bitsaver s_tidataBookVol2_45945 352/page/n1217) SN74LS601A (https://arc hive.org/details/bitsaver s_tidataBookVol2_45945 352/page/n1217) SN74LS603A (https://arc hive.org/details/bitsaver s_tidataBookVol2_45945 352/page/n1217) SN74LS603A (https://arc hive.org/details/bitsaver s_tidataBookVol2_45945 352/page/n1217) SN74LS604 (https://arch ive.org/details/bitsavers s_tidataBookVol2_459453 352/page/n1217) SN74LS604 (https://arch ive.org/details/bitsavers s_tidataBookVol2_459453 352/page/n1225)

					_tidataBookVol2_459453 52/page/n1225)
74x606	1	octal 2-input multiplexer, latch, glitch-free	three- state	28	SN74LS606 (https://arch ive.org/details/bitsavers _tidataBookVol2_459453 52/page/n1225)
74x607	1	octal 2-input multiplexer, latch, glitch-free	open- collector	28	SN74LS607 (https://arch ive.org/details/bitsavers _tidataBookVol2_459453 52/page/n1225)
74x608	1	memory cycle controller		16	SN74LS608 (https://arch ive.org/details/bitsavers _tidataBookVol2_459453 52/page/n1231)
74x610	1	memory mapper, latched	three- state	40	SN74LS610 (https://arch ive.org/details/bitsavers _tidataBookVol2_459453 52/page/n1237)
74x611	1	memory mapper, latched	open- collector	40	SN74LS611 (https://arch ive.org/details/bitsavers _tidataBookVol2_459453 52/page/n1237)
74x612	1	memory mapper	three- state	40	SN74LS612 (https://arch ive.org/details/bitsavers _tidataBookVol2_459453 52/page/n1237)
74x613	1	memory mapper	open- collector	40	SN74LS613 (https://arch ive.org/details/bitsavers _tidataBookVol2_459453 52/page/n1237)
74x614	1	octal bus transceiver and register, inverting	open- collector	24	SN74ALS614 (https://ar chive.org/details/bitsave rs_tidataBooktaBook_60 160366/page/n495)
74x615	1	octal bus transceiver and register, non-inverting	open- collector	24	SN74ALS615 (https://ar chive.org/details/bitsave rs_tidataBooktaBook_60 160366/page/n495)
74x616	1	16-bit parallel error detection and correction	three- state	40	SN74ALS616 (https://ar chive.org/details/bitsave rs_tidataBook_2834648 4/page/n101)
74x617	1	16-bit parallel error detection and correction	open- collector	40	SN74ALS617 (https://ar chive.org/details/bitsave rs_tidataBook_2834648 4/page/n101)
74x620	1	octal bus transceiver, inverting	three- state	20	SN74LS620 (http://www. ti.com/lit/gpn/sn74ls623)
74x621	1	octal bus transceiver, non- inverting	open- collector	20	SN74LS621 (http://www. ti.com/lit/gpn/sn74ls623)
74x622	1	octal bus transceiver, inverting	open- collector	20	SN74LS622 (https://arch ive.org/details/bitsavers _tidataBookVol2_459453 52/page/n1247)

74x623	1	octal bus transceiver, non- inverting		three- state	20	SN74LS623 (http://www. ti.com/lit/gpn/sn74ls623)
74x624	1	voltage-controlled oscillator, enable control, range control, two-phase outputs	analog		14	SN74LS624 (http://www. ti.com/lit/gpn/sn74ls624)
74x625	2	dual voltage-controlled oscillator, two-phase outputs	analog		16	SN74LS625 (http://www. ti.com/lit/gpn/sn74ls624)
74x626	2	dual voltage-controlled oscillator, enable control, two-phase outputs	analog		16	SN74LS626 (http://www. ti.com/lit/gpn/sn74ls624)
74x627	2	dual voltage-controlled oscillator	analog		14	SN74LS627 (http://www. ti.com/lit/gpn/sn74ls624)
74x628	1	voltage-controlled oscillator, enable control, range control, external temperature compensation, two-phase outputs	analog		14	SN74LS628 (http://www. ti.com/lit/gpn/sn74ls624)
74x629	2	dual voltage-controlled oscillator, enable control, range control	analog		16	SN74LS629 (http://www. ti.com/lit/gpn/sn74ls624)
74x630	1	16-bit error detection and correction (EDAC)		three- state	28	SN74LS630 (https://arch ive.org/details/bitsavers _tidataBookVol2_459453 52/page/n1263)
74x631	1	16-bit error detection and correction		open- collector	28	SN74LS631 (https://arch ive.org/details/bitsavers _tidataBookVol2_459453 52/page/n1263)
74x632	1	32-bit parallel error detection and correction, byte-write		three- state	52	SN74ALS632 (https://ar chive.org/details/bitsave rs_tidataBookVol3_2584 0031/page/n457)
74x633	1	32-bit parallel error detection and correction, byte-write		open- collector	52	SN74ALS633 (https://ar chive.org/details/bitsave rs_tidataBookVol3_2584 0031/page/n457)
74x634	1	32-bit parallel error detection and correction		three- state	48	SN74ALS634 (https://ar chive.org/details/bitsave rs_tidataBookVol3_2584 0031/page/n457)
74x635	1	32-bit parallel error detection and correction		open- collector	48	SN74ALS635 (https://ar chive.org/details/bitsave rs_tidataBookVol3_2584 0031/page/n457)
74x636	1	8-bit parallel error detection and correction		three- state	20	SN74LS636 (https://arch ive.org/details/bitsavers _tidataBookVol2_459453 52/page/n1271)
74x637	1	8-bit parallel error detection and correction		open- collector	20	SN74LS637 (https://arch ive.org/details/bitsavers _tidataBookVol2_459453 52/page/n1271)
74x638	1	octal bus transceiver, inverting outputs		three- state	20	SN74LS638 (https://arch ive.org/details/bitsavers

			and open- collector		_tidataBookVol2_459453 52/page/n1279)
74x639	1	octal bus transceiver, non- inverting outputs	three- state and open- collector	20	SN74LS639 (https://arch ive.org/details/bitsavers _tidataBookVol2_459453 52/page/n1279)
74x640	1	octal bus transceiver, inverting outputs	three- state	20	SN74LS640 (http://www. ti.com/lit/gpn/sn74ls640)
74x641	1	octal bus transceiver, non- inverting outputs	open- collector	20	SN74LS641 (http://www. ti.com/lit/gpn/sn74ls640)
74x642	1	octal bus transceiver, inverting outputs	open- collector	20	SN74LS642 (http://www. ti.com/lit/gpn/sn74ls640)
74x643	1	octal bus transceiver, mix of inverting and non-inverting outputs	three- state	20	SN74LS643 (https://arch ive.org/details/bitsavers _tidataBookVol2_459453 52/page/n1283)
74x644	1	octal bus transceiver, mix of inverting and non-inverting outputs	open- collector	20	SN74LS644 (http://www. ti.com/lit/gpn/sn74ls640)
74x645	1	octal bus transceiver, non- inverting outputs	three- state	20	SN74LS645 (http://www. ti.com/lit/gpn/sn74ls640)
74x646	1	octal bus transceiver/latch/multiplexer, non-inverting outputs	three- state	24	SN74ALS646A (http://w ww.ti.com/lit/gpn/sn54al s648)
74x647	1	octal bus transceiver/latch/multiplexer, non-inverting outputs	open- collector	24	SN74LS647 (https://arch ive.org/details/bitsavers _tidataBookVol2_459453 52/page/n1291)
74x648	1	octal bus transceiver/latch/multiplexer, inverting outputs	three- state	24	SN74ALS648A (http://w ww.ti.com/lit/gpn/sn54al s648)
74x649	1	octal bus transceiver/latch/multiplexer, inverting outputs	open- collector	24	SN74LS649 (https://arch ive.org/details/bitsavers _tidataBookVol2_459453 52/page/n1291)
74x651	1	octal bus transceiver/register, inverting outputs	three- state	24	SN74ALS651A (http://w ww.ti.com/lit/gpn/sn74al s654)
74x652	1	octal bus transceiver/register, non- inverting outputs	three- state	24	SN74ALS652A (http://w ww.ti.com/lit/gpn/sn74al s654)
74x653	1	octal bus transceiver/register, inverting outputs	three- state and open- collector	24	SN74ALS653 (http://ww w.ti.com/lit/gpn/sn74als6 54)
74x654	1	octal bus transceiver/register, non- inverting outputs	three- state and open- collector	24	SN74ALS654 (http://ww w.ti.com/lit/gpn/sn74als6 54)

74x655	1	octal buffer / line driver with parity, inverting	three state	- 24	74F655 (https://archive. org/details/bitsavers_fair childdldFASTDataBook_ 29981933/page/n553)
74x656	1	octal buffer / line driver with parity, non-inverting	three state	- 24	74F656 (https://archive. org/details/bitsavers_fair childdldFASTDataBook_ 29981933/page/n553)
74x657	1	octal bidirectional transceiver with 8-bit parity generator/checker	three state	- 24	SN74F657 (http://www.ti. com/lit/gpn/sn74f657)
74x658	1	octal bus transceiver, parity, inverting	three state	- 24	SN74HC658 (https://arc hive.org/details/bitsaver s_tidataBookogicDataBo ok_23574286/page/n39 5)
74x659	1	octal bus transceiver, parity, non-inverting	three state	- 24	SN74HC659 (https://arc hive.org/details/bitsaver s_tidataBookogicDataBo ok_23574286/page/n39 5)
74x664	1	octal bus transceiver, parity, inverting	three state	- 24	SN74HC664 (https://arc hive.org/details/bitsaver s_tidataBookogicDataBo ok_23574286/page/n40 9)
74x665	1	octal bus transceiver, parity, non-inverting	three state	24	SN74HC665 (https://arc hive.org/details/bitsaver s_tidataBookogicDataBo ok_23574286/page/n40 9)
74x666	1	8-bit D-type transparent read- back latch, non-inverting	three state	- 24	SN74ALS666 (http://ww w.ti.com/lit/gpn/sn74als6 66)
74x667	1	8-bit D-type transparent read- back latch, inverting	three state	- 24	SN74ALS667 (http://ww w.ti.com/lit/gpn/sn74als6 66)
74x668	1	synchronous 4-bit decade up/down counter		16	SN74LS668 (https://we b.archive.org/web/20060 602131759/http://focus.t i.com/lit/ds/symlink/sn7 4ls669.pdf)
74x669	1	synchronous 4-bit binary up/down counter		16	SN74LS669 (https://we b.archive.org/web/20060 602131759/http://focus.t i.com/lit/ds/symlink/sn7 4ls669.pdf)
74x670	1	16-bit register file (4x4)	three state	- 16	SN74LS670 (http://www. ti.com/lit/gpn/sn54ls670)
74x671	1	4-bit bidirectional shift register/latch/multiplexer, direct clear	three state	- 20	SN74LS671 (https://arch ive.org/details/bitsavers _tidataBookVol2_459453 52/page/n1327)
74x672	1	4-bit bidirectional shift register/latch/multiplexer, synchronous clear	three state	- 20	SN74LS672 (https://arch ive.org/details/bitsavers

						_tidataBookVol2_459453 52/page/n1327)
74x673	1	16-bit serial-in, serial/parallel- out shift register, output storage registers		three- state	24	SN74LS673 (http://www. ti.com/lit/gpn/sn74ls673)
74x674	1	16-bit parallel-in, serial-out shift register		three- state	24	SN74LS674 (http://www. ti.com/lit/gpn/sn74ls673)
74x675	1	16-bit serial-in, serial/parallel- out shift register			24	74F675A (https://archiv e.org/stream/NationalSe miconductor1988FASTA dvancedSchottkyDatabo ok/National%20Semicon ductor%201988%20FAS T%20Advanced%20Sch ottky%20Databook#pag e/n607)
74x676	1	16-bit serial/parallel-in, serial- out shift register			24	74F676 (https://archive. org/stream/NationalSemi conductor1988FASTAdv ancedSchottkyDataboo k/National%20Semicond uctor%201988%20FAS T%20Advanced%20Sch ottky%20Databook#pag e/n611)
74x677	1	16-bit address <u>comparator,</u> enable			24	SN74ALS677 (https://ar chive.org/details/bitsave rs_tidataBookVol3_2584 0031/page/n507)
74x678	1	16-bit address comparator, latch			24	SN74ALS678 (https://ar chive.org/details/bitsave rs_tidataBookVol3_2584 0031/page/n507)
74x679	1	12-bit address comparator, latch			20	SN74ALS679 (https://ar chive.org/details/bitsave rs_tidataBookVol3_2584 0031/page/n513)
74x680	1	12-bit address comparator, enable			20	SN74ALS680 (https://ar chive.org/details/bitsave rs_tidataBookVol3_2584 0031/page/n513)
74x681	1	4-bit parallel binary accumulator		three- state	20	SN74LS681 (https://arch ive.org/details/bitsavers _tidataBookVol2_459453 52/page/n1339)
74x682	1	8-bit <u>magnitude comparator,</u> P>Q output	20 kΩ pull-up		20	SN74LS682 (https://we b.archive.org/web/20160 531200122/http://www.ti. com/lit/ds/symlink/sn74l s682.pdf)
74x683	1	8-bit magnitude comparator, P>Q output	20 kΩ pull-up	open- collector	20	SN74LS683 (https://arch ive.org/details/bitsavers _tidataBookVol2_459453 52/page/n1345)
74x684	1	8-bit magnitude comparator, P>Q output			20	SN74LS684 (https://we b.archive.org/web/20160 531200122/http://www.ti.

					com/lit/ds/symlink/sn74l s682.pdf)
74x685	1	8-bit magnitude comparator, P>Q output	open- collector	20	SN74LS685 (https://we b.archive.org/web/20160 531200122/http://www.ti. com/lit/ds/symlink/sn74l s682.pdf)
74x686	1	8-bit magnitude comparator, P>Q output, enable		24	SN74LS686 (https://we b.archive.org/web/20160 531200122/http://www.ti. com/lit/ds/symlink/sn74l s682.pdf)
74x687	1	8-bit magnitude comparator, P>Q output, enable	open- collector	24	SN74LS687 (https://we b.archive.org/web/20160 531200122/http://www.ti. com/lit/ds/symlink/sn74l s682.pdf)
74x688	1	8-bit magnitude comparator, enable		20	SN74LS688 (https://we b.archive.org/web/20160 531200122/http://www.ti. com/lit/ds/symlink/sn74l s682.pdf)
74x689	1	8-bit magnitude comparator, enable	open- collector	20	SN74LS689 (https://arch ive.org/details/bitsavers _tidataBookVol2_459453 52/page/n1345)
74x690	1	4-bit decimal counter/latch/multiplexer, asynchronous clear	three- state	20	SN74LS690 (https://arch ive.org/details/bitsavers _tidataBookVol2_459453 52/page/n1353)
74x691	1	4-bit binary counter/latch/multiplexer, asynchronous clear	three- state	20	SN74LS691 (https://arch ive.org/details/bitsavers _tidataBookVol2_459453 52/page/n1353)
74x692	1	4-bit decimal counter/latch/multiplexer, synchronous clear	three- state	20	SN74LS692 (https://arch ive.org/details/bitsavers _tidataBookVol2_459453 52/page/n1353)
74x693	1	4-bit binary counter/latch/multiplexer, synchronous clear	three- state	20	SN74LS693 (https://arch ive.org/details/bitsavers _tidataBookVol2_459453 52/page/n1353)
74x694	1	4-bit decimal counter/latch/multiplexer, synchronous and asynchronous clears	three- state	20	SN74ALS694 (https://ar chive.org/details/bitsave rs_icMaster19_1595694 96/page/n619)
74x695	1	4-bit binary counter/latch/multiplexer, synchronous and asynchronous clears	three- state	20	SN74ALS695 (https://ar chive.org/details/bitsave rs_icMaster19_1595694 96/page/n619)
74x696	1	4-bit decimal counter/register/multiplexer, asynchronous clear	three- state	20	SN74LS696 (http://www. ti.com/lit/gpn/sn74ls697)
74x697	1	4-bit binary counter/register/multiplexer, asynchronous clear	three- state	20	SN74LS697 (http://www. ti.com/lit/gpn/sn74ls697)

74x698	1	4-bit decimal counter/register/multiplexer, synchronous clear		three- state	20	SN74LS698 (https://arch ive.org/details/bitsavers _tidataBookVol2_459453 52/page/n1365)
74x699	1	4-bit binary counter/register/multiplexer, synchronous clear		three- state	20	SN74LS699 (http://www. ti.com/lit/gpn/sn74ls697)
Part number	Units	Description	Input	Output	Pins	Datasheet
74x700	1	octal dRAM driver, inverting		three- state	20	SN74S700 (https://archi ve.org/stream/Monolithic Memories-MMI-BipolarL SI1984DatabookOCR#p age/n315)
74x701	1	8-bit register/counter/comparator		three- state	24	74F701 (https://archive. org/stream/NationalSemi conductor1988FASTAdv ancedSchottkyDataboo k/National%20Semicond uctor%201988%20FAS T%20Advanced%20Sch ottky%20Databook#pag e/n615)
74x702	1	8-bit registered read-back transceiver		three- state	24	74F702 (https://archive. org/stream/NationalSemi conductor1988FASTAdv ancedSchottkyDataboo k/National%20Semicond uctor%201988%20FAS T%20Advanced%20Sch ottky%20Databook#pag e/n617)
74x705	1	arithmetic logic unit for digital signal processing applications		three- state	(84)	74ACT705 (https://archi ve.org/details/bitsavers_ fairchilddldFACTLogicDa taBook_27153725/page/ n349)
74x707	1	8-bit TTL-ECL shift register			20	74F707 (https://archive. org/details/bitsavers_nat ionaldaFASTDatabook_3 1226275/page/n621)
74x708	1	576-bit FIFO memory (64x9)		three- state	28	74ACT708 (https://archi ve.org/details/bitsavers_ fairchilddldFACTLogicDa taBook_27153725/page/ n361)
74x710	1	8-bit single-supply TTL-ECL shift register			20	74F710 (https://archive. org/stream/NationalSemi conductor1988FASTAdv ancedSchottkyDataboo k/National%20Semicond uctor%201988%20FAS T%20Advanced%20Sch ottky%20Databook#pag e/n621)
74x711	5	quint 2-to-1 multiplexers		three- state	20	74F711 (https://archive. org/details/bitsavers_sig neticsdaManual_579666 40/page/n777)

74x712	5	quint 3-to-1 multiplexers			24	74F712 (https://archive. org/details/bitsavers_sig neticsdaManual_579666 40/page/n777)
74x715	1	programmable video sync generator			20	74ACT715 (https://datas heet.datasheetarchive.c om/originals/distributors/ Datasheets-303/53948.p df)
74x716	1	programmable decade counter			16	SN74LS716 (https://arch ive.org/details/bitsavers _motoroladaSchottkyTT LData_33878952/page/n 397)
74x718	1	programmable binary counter			16	SN74LS718 (https://arch ive.org/details/bitsavers _motoroladaSchottkyTT LData_33878952/page/n 397)
74x723	1	576-bit FIFO memory (64x9)		three- state	28	74ACT723 (https://archi ve.org/details/bitsavers_ fairchilddldFACTLogicDa taBook_27153725/page/ n379)
74x724	1	voltage-controlled multivibrator	analog		8	SN74LS724 (https://arch ive.org/details/bitsavers _motoroladaSchottkyTT LData_33878952/page/n 409)
74x725	1	4608-bit FIFO memory (512x9)		three- state	28	74ACT725 (https://archi ve.org/details/bitsavers_ fairchilddldFACTLogicDa taBook_27153725/page/ n395)
74x730	1	octal dRAM driver, inverting		three- state	20	SN74S730 (https://archi ve.org/stream/Monolithic Memories-MMI-BipolarL SI1984DatabookOCR#p age/n315)
74x731	1	octal dRAM driver, non- inverting		three- state	20	SN74S731 (https://archi ve.org/stream/Monolithic Memories-MMI-BipolarL SI1984DatabookOCR#p age/n315)
74x732	1	4-bit 3-bus multiplexer, inverting		three- state	20	74F732 (https://archive. org/details/bitsavers_sig neticsdaManual_579666 40/page/n789)
74x733	1	4-bit 3-bus multiplexer, non- inverting		three- state	20	74F733 (https://archive. org/details/bitsavers_sig neticsdaManual_579666 40/page/n789)
74x734	1	octal dRAM driver, non- inverting		three- state	20	SN74S734 (https://archi ve.org/stream/Monolithic Memories-MMI-BipolarL SI1984DatabookOCR#p age/n315)

74x740	2	dual 4-bit line driver, inverting		three- state	20	SN74S740 (https://datas heet.datasheetarchive.c om/originals/scans/Scan s-056/DSAIH000137088. pdf)
74x741	2	dual 4-bit line driver, non- inverting, complementary enable inputs		three- state	20	SN74S741 (https://datas heet.datasheetarchive.c om/originals/scans/Scan s-056/DSAIH000137088. pdf)
74x742	1	octal line driver, inverting		open- collector	20	SN74ALS742 ^{[10]:3-122} [11]:25
74x743	1	octal line driver, non-inverting		open- collector	20	SN74ALS743 ^{[10]:3-124} [11]:25
74x744	2	dual 4-bit line driver, non- inverting		three- state	20	SN74S744 (https://datas heet.datasheetarchive.c om/originals/scans/Scan s-056/DSAIH000137088. pdf)
74x746	1	octal buffer / line driver, inverting	20 kΩ pull-up	three- state	20	SN74ALS746 (https://ar chive.org/details/bitsave rs_tidataBooktaBook_60 160366/page/n623)
74x747	1	octal buffer / line driver, non- inverting	20 kΩ pull-up	three- state	20	SN74ALS747 (https://ar chive.org/details/bitsave rs_tidataBooktaBook_60 160366/page/n623)
74x748	1	8 to 3-line priority encoder (glitch-less)			16	SN74LS748 (https://arch ive.org/details/bitsavers _motoroladaSchottkyTT LData_33878952/page/n 151)
74x756	1	octal buffer/line driver, inverting outputs		open- collector	20	SN74AS756 (http://www. ti.com/lit/gpn/sn54as75 6)
74x757	1	octal buffer/line driver, non- inverting outputs, complementary enable inputs		open- collector	20	SN74AS757 (http://www. ti.com/lit/gpn/sn54as75 6)
74x758	1	quadruple bus transceivers, inverting outputs		open- collector	14	SN74AS758 (https://arc hive.org/details/bitsaver s_tidataBookVol3_25840 031/page/n527)
74x759	1	quadruple bus transceivers, non-inverting outputs		open- collector	14	SN74AS759 (https://arc hive.org/details/bitsaver s_tidataBookVol3_25840 031/page/n527)
74x760	1	octal buffer/line driver, non- inverting outputs		open- collector	20	SN74ALS760 (http://ww w.ti.com/lit/gpn/sn54as7 60)
74x762	1	octal buffer/line driver, inverting and non-inverting outputs		open- collector	20	SN74ALS762 (https://we b.archive.org/web/20170 224211619/http://www.ti. com/lit/ds/symlink/sn74 as762.pdf)

74x763	1	octal buffer/line driver, inverting outputs, complementary enable inputs	open- collector	20	SN74ALS763 (https://we b.archive.org/web/20170 224211619/http://www.ti. com/lit/ds/symlink/sn74 as762.pdf)
74x764	1	dual-port dRAM controller		40	74F764 (https://archive. org/details/bitsavers_sig neticsdaManual_579666 40/page/n795)
74x765	1	dual-port dRAM controller with address latch		40	74F765 (https://archive. org/details/bitsavers_sig neticsdaManual_579666 40/page/n795)
74x776	1	8-bit latched transceiver for <u>FutureBus</u>	three- state and open- collector	28	SN74F776 (https://archi ve.org/details/TexasInstr uments-TI-Data-Advanc edLogicandBusInterface Logic1991OCR/page/n45 3)
74x777	3	triple latched transceiver	three- state and open- collector	20	74F777 (https://cdn.data sheetspdf.com/pdf-dow n/7/4/F/74F777_PhilipsS emiconductors.pdf)
74x779	1	8-bit bidirectional binary counter	three- state	16	MC74F779 (https://archi ve.org/details/bitsavers_ motoroladaFASTandLST TLData_35934218/page/ n297)
74x783	1	synchronous address multiplexer for display systems		40	SN74LS783 (https://arch ive.org/details/bitsavers _motoroladaSchottkyTT LData_33878952/page/n 411)
74x784	1	8-bit serial/parallel multiplier with adder/subtractor		20	74F784 (https://archive. org/details/bitsavers_fair childdldFASTDataBook_ 29981933/page/n583)
74x785	1	synchronous address multiplexer for display systems with 256-column refresh		40	SN74LS785 (https://cdn. datasheetspdf.com/pdf-d own/S/N/7/SN74LS783_ MotorolaSemiconductor. pdf)
74x786	1	4-input asynchronous bus arbiter		16	74F786 (https://archive. org/details/bitsavers_sig neticsdaManual_579666 40/page/n835)
74x790	1	error detection and correction (EDAC)	three- state	48	SN74ALS790 (https://ar chive.org/details/bitsave rs_motoroladaSchottkyT TLData_33878952/page/ n629)
74x793	1	8-bit latch, readback		20	SN74LS793 (https://arch ive.org/stream/Monolithi cMemories-MMI-Bipolar LSI1984DatabookOCR# page/n433)

74x794	1	8-bit register, readback			20	SN74LS794 (https://arch ive.org/stream/Monolithi cMemories-MMI-Bipolar LSI1984DatabookOCR# page/n433)
74x795	1	octal buffer, non-inverting, common enable		three- state	20	SN74LS795 (https://arch ive.org/details/bitsavers _motoroladaSchottkyTT LData_33878952/page/n 437)
74x796	1	octal buffer, inverting, common enable		three- state	20	SN74LS796 (https://arch ive.org/details/bitsavers _motoroladaSchottkyTT LData_33878952/page/n 437)
74x797	1	octal buffer, non-inverting, enable for 4 buffers each		three- state	20	SN74LS797 (https://arch ive.org/details/bitsavers _motoroladaSchottkyTT LData_33878952/page/n 437)
74x798	1	octal buffer, inverting, enable for 4 buffers each		three- state	20	SN74LS798 (https://arch ive.org/details/bitsavers _motoroladaSchottkyTT LData_33878952/page/n 437)
Part number	Units	Description	Input	Output	Pins	Datasheet
74×900	2	triple 4-input AND/NAND		driver	20	SN74AS800 (https://arc hive.org/details/bitsaver
74x800	5	drivers		unver	20	s_tidataBookVol3_25840 031/page/n537)
74x800	3	drivers triple 4-input OR/NOR drivers		driver	20	s_tidataBookVol3_25840 031/page/n537) SN74AS802 (https://arc hive.org/details/bitsaver s_tidataBookVol3_25840 031/page/n541)
74x800 74x802 74x803	3	drivers triple 4-input OR/NOR drivers quad D flip flops with matched propagation delays		driver	20	s_tidataBookVol3_25840 031/page/n537) SN74AS802 (https://arc hive.org/details/bitsaver s_tidataBookVol3_25840 031/page/n541) MC74F803 (https://archi ve.org/details/bitsavers_ motoroladaFASTandLST TLData_35934218/page/ n301)
74x800 74x802 74x803 74x804	3 4 6	drivers triple 4-input OR/NOR drivers quad D flip flops with matched propagation delays hex 2-input NAND drivers		driver	20 20 14 20	s_tidataBookVol3_25840 031/page/n537) SN74AS802 (https://arc hive.org/details/bitsaver s_tidataBookVol3_25840 031/page/n541) MC74F803 (https://archi ve.org/details/bitsavers_ motoroladaFASTandLST TLData_35934218/page/ n301) SN74ALS804A (http://w ww.ti.com/lit/gpn/sn54as 804b)
74x800 74x802 74x803 74x804 74x805	3 3 4 6 6	drivers triple 4-input OR/NOR drivers quad D flip flops with matched propagation delays hex 2-input NAND drivers hex 2-input NOR drivers		driver driver driver	20 20 14 20 20	s_tidataBookVol3_25840 031/page/n537) SN74AS802 (https://arc hive.org/details/bitsaver s_tidataBookVol3_25840 031/page/n541) MC74F803 (https://archi ve.org/details/bitsavers_ motoroladaFASTandLST TLData_35934218/page/ n301) SN74ALS804A (http://w ww.ti.com/lit/gpn/sn54as 804b) SN74ALS805A (http://w ww.ti.com/lit/gpn/sn54as 805b)
74x800 74x802 74x803 74x804 74x805 74x807	3 3 4 6 6 1	drivers triple 4-input OR/NOR drivers quad D flip flops with matched propagation delays hex 2-input NAND drivers hex 2-input NOR drivers 1-to-10 clock driver		driver driver driver driver	20 20 14 20 20 20	s_tidataBookVol3_25840 031/page/n537) SN74AS802 (https://arc hive.org/details/bitsaver s_tidataBookVol3_25840 031/page/n541) MC74F803 (https://archi ve.org/details/bitsavers_ motoroladaFASTandLST TLData_35934218/page/ n301) SN74ALS804A (http://w ww.ti.com/lit/gpn/sn54as 804b) SN74ALS805A (http://w ww.ti.com/lit/gpn/sn54as 805b) IDT74FCT807 (https://ar chive.org/details/bitsave rs_idtdataBoomanceLogi cDataBook_51362967/p age/n569)
74x800 74x802 74x803 74x804 74x805 74x807 74x808	3 3 4 6 1 6	drivers triple 4-input OR/NOR drivers quad D flip flops with matched propagation delays hex 2-input NAND drivers hex 2-input NOR drivers 1-to-10 clock driver hex 2-input AND drivers		driver driver driver driver driver	20 20 14 20 20 20 20	s_tidataBookVol3_25840 031/page/n537) SN74AS802 (https://arc hive.org/details/bitsaver s_tidataBookVol3_25840 031/page/n541) MC74F803 (https://archi ve.org/details/bitsavers_ motoroladaFASTandLST TLData_35934218/page/ n301) SN74ALS804A (http://w ww.ti.com/lit/gpn/sn54as 804b) SN74ALS805A (http://w ww.ti.com/lit/gpn/sn54as 805b) IDT74FCT807 (https://ar chive.org/details/bitsave rs_idtdataBoomanceLogi cDataBook_51362967/p age/n569) SN74AS808B (http://ww w.ti.com/lit/gpn/sn74as8 08b)

					com/lit/ds/symlink/sn74 als810.pdf)
74x811	4	quad 2-input XNOR gates	open- collector	14	DM74ALS811 (https://ar chive.org/details/bitsave rs_nationaldaicDatabook _22808448/page/n349)
74x817	1	GTL+ to LV-TTL 1-to-6 fanout / LV-TTL to GTL+ 1- to-2 fanout driver	three- state and open- collector	(24)	SN74GTLP817 (https:// www.ti.com/lit/gpn/SN74 GTLP817)
74x818	1	8-bit diagnostic register	three- state	24	74ACT818 (https://archi ve.org/details/bitsavers_ fairchilddldFACTLogicDa taBook_27153725/page/ n411)
74x819	1	8-bit diagnostic / pipeline register	three- state	24	SN74ALS819 (https://pd f1.alldatasheet.com/data sheet-pdf/view/466541/T I1/SN74ALS819.html)
74x821	1	10-bit bus interface flip-flop	three- state	24	SN74AS821A (http://ww w.ti.com/lit/gpn/sn54as8 21a)
74x822	1	10-bit bus interface flip-flop, inverting inputs	three- state	24	SN74AS822 (https://arc hive.org/details/bitsaver s_tidataBookVol3_25840 031/page/n557)
74x823	1	9-bit D-type flip-flops, clear and clock enable inputs	three- state	24	SN74AS823A (http://ww w.ti.com/lit/gpn/sn54as8 23a)
74x824	1	9-bit D-type flip-flops, clear and clock enable inputs, inverting inputs	three- state	24	SN74AS824 (https://arc hive.org/details/bitsaver s_tidataBookVol3_25840 031/page/n563)
74x825	1	8-bit D-type flip-flop, clear and clock enable inputs	three- state	24	SN74AS825A (http://ww w.ti.com/lit/gpn/sn54as8 25a)
74x826	1	8-bit D-type flip-flop, clear and clock enable inputs, inverting inputs	three- state	24	SN74AS826 (https://arc hive.org/details/bitsaver s_tidataBookVol3_25840 031/page/n569)
74x827	1	10-bit buffer, non-inverting	three- state	24	MC74F827 (https://archi ve.org/details/bitsavers_ motoroladaFASTandLST TLData_35934218/page/ n303)
74x828	1	10-bit buffer, inverting	three- state	24	MC74F828 (https://archi ve.org/details/bitsavers_ motoroladaFASTandLST TLData_35934218/page/ n303)
74x832	6	hex 2-input OR drivers	driver	20	SN74ALS832A (https://w eb.archive.org/web/2017 0221112630/http://www.t i.com/lit/ds/symlink/sn7 4als832a.pdf)

74x833	1	8-bit to 9-bit bus transceiver with parity register, non- inverting	three- state	24	SN74ABT833 (http://ww w.ti.com/lit/gpn/sn74abt8 33)
74x834	1	8-bit to 9-bit bus transceiver with parity register, inverting	three- state	24	IDT74FCT834 (https://ar chive.org/details/bitsave rs_idtdataBoomanceCM OSDataBook_66222191/ page/n1071)
74x835	1	8-bit shift register with 2:1 input multiplexers, one input latched, serial output		24	74F835 (https://cdn.data sheetspdf.com/pdf-dow n/7/4/F/74F835_PhilipsS emiconductors.pdf)
74x839	1	field-programmable logic array 14x32x6	three- state	24	SN74PL839 (https://arch ive.org/details/TexasInst ruments-TI-Data-TtIData BookVol1_1984-DL/pag e/n259)
74x840	1	field-programmable logic array 14x32x6	open- collector	24	SN74PL840 (https://arch ive.org/details/TexasInst ruments-TI-Data-TtIData BookVol1_1984-DL/pag e/n259)
74x841	1	10-bit D-type flip-flop	three- state	24	SN74ALS841 (https://we b.archive.org/web/20170 225141931/http://www.ti. com/lit/ds/symlink/sn74 als841.pdf)
74x842	1	10-bit D-type flip-flop, inverting inputs	three- state	24	SN74ALS842 (https://ar chive.org/details/bitsave rs_tidataBookVol3_2584 0031/page/n579)
74x843	1	9-bit D flip-flops, clear and set inputs	three- state	24	SN74ALS843 (http://ww w.ti.com/lit/gpn/sn74als8 43)
74x844	1	9-bit D flip-flops, clear and set inputs, inverting inputs	three- state	24	SN74ALS844 (https://ar chive.org/details/bitsave rs_tidataBookVol3_2584 0031/page/n587)
74x845	1	8-bit D flip-flops, clear and set inputs	three- state	24	SN74ALS845 (https://ar chive.org/details/bitsave rs_tidataBookVol3_2584 0031/page/n595)
74x846	1	8-bit D flip-flops, clear and set inputs, inverting inputs	three- state	24	SN74ALS846 (https://ar chive.org/details/bitsave rs_tidataBookVol3_2584 0031/page/n595)
74x848	1	8 to 3-line priority encoder (glitch-less)	three- state	16	SN74LS848 (https://arch ive.org/details/bitsavers _motoroladaSchottkyTT LData_33878952/page/n 315)
74x850	1	1 of 16 data selector/multiplexer, clocked select	three- state	28	SN74AS850 (https://arc hive.org/details/bitsaver s_tidataBookVol3_25840 031/page/n603)

74x851	1	1 of 16 data selector/multiplexer	three- state	28	SN74AS851 (https://arc hive.org/details/bitsaver s_tidataBookVol3_25840 031/page/n603)
74x852	1	8-bit universal transceiver port controller	three- state	24	SN74AS852 (https://arc hive.org/details/bitsaver s_tidataBookVol3_25840 031/page/n613)
74x853	1	8-bit to 9-bit bus transceiver with parity latch, non- inverting	three- state	24	SN74ABT853 (http://ww w.ti.com/lit/gpn/sn74abt8 53)
74x854	1	8-bit to 9-bit bus transceiver with parity latch, inverting	three- state	24	IDT74FCT854 (https://ar chive.org/details/bitsave rs_idtdataBoomanceCM OSDataBook_66222191/ page/n1071)
74x856	1	8-bit universal transceiver port controller	three- state	24	SN74AS856 (https://arc hive.org/details/bitsaver s_tidataBookVol3_25840 031/page/n619)
74x857	6	hex 2-line to 1-line multiplexer	three- state	24	SN74ALS857 (http://ww w.ti.com/lit/gpn/sn54als8 57)
74x861	1	10-bit bus transceiver, non- inverting	three- state	24	SN74ABT861 (https://ar chive.org/details/bitsave rs_tidataBook_8079374 0/page/n263)
74x862	1	10-bit bus transceiver, inverting	three- state	24	SN74ABT862 (https://ar chive.org/details/bitsave rs_tidataBook_8079374 0/page/n269)
74x863	1	9-bit bus transceiver, non- inverting	three- state	24	SN74ABT863 (https://ar chive.org/details/bitsave rs_tidataBook_8079374 0/page/n273)
74x864	1	9-bit bus transceiver, inverting	three- state	24	74F864 (https://archive. org/details/bitsavers_sig neticsdaManual_579666 40/page/n867)
74x866	1	8-bit magnitude comparator with latches		24	SN74AS866 (https://arc hive.org/details/bitsaver s_tidataBookVol3_25840 031/page/n633)
74x867	1	synchronous 8-bit up/down counter, asynchronous clear		24	SN74ALS867A (http://w ww.ti.com/lit/gpn/sn74al s867a)
74x869	1	synchronous 8-bit up/down counter, synchronous clear		24	SN74ALS869 (http://ww w.ti.com/lit/gpn/sn74als8 67a)
74x870	1	dual 16x4 register files		24	SN74AS870 (https://arc hive.org/details/bitsaver s_tidataBookVol3_25840 031/page/n645)
74x871	1	dual 16x4 register files		28	SN74AS871 (https://arc hive.org/details/bitsaver

					s_tidataBookVol3_25840 031/page/n645)
74x873	2	dual 4-bit transparent latch with clear	three- state	24	SN74ALS873B (http://w ww.ti.com/lit/gpn/sn74al s873b)
74x874	2	dual 4-bit edge-triggered D flip-flops with clear	three- state	24	SN74ALS874 (http://ww w.ti.com/lit/gpn/sn74as8 74)
74x876	2	dual 4-bit edge-triggered D flip-flops with set, inverting outputs	three- state	24	SN74ALS876 (http://ww w.ti.com/lit/gpn/sn74as8 74)
74x877	1	8-bit universal transceiver port controller	three- state	24	SN74AS877 (https://arc hive.org/details/bitsaver s_tidataBookVol3_25840 031/page/n663)
74x878	2	dual 4-bit D-type flip-flop, synchronous clear, non- inverting outputs	three- state	24	SN74ALS878 (https://ar chive.org/details/bitsave rs_tidataBookVol3_2584 0031/page/n669)
74x879	2	dual 4-bit D-type flip-flop, synchronous clear, inverting outputs	three- state	24	SN74ALS879 (https://ar chive.org/details/bitsave rs_tidataBookVol3_2584 0031/page/n669)
74x880	2	dual 4-bit transparent latch with clear, inverting outputs	three- state	24	SN74ALS880 (https://ar chive.org/details/bitsave rs_tidataBookVol3_2584 0031/page/n675)
74x881	1	4-bit arithmetic logic unit		24	SN74AS881A (https://ar chive.org/details/bitsave rs_tidataBookVol3_2584 0031/page/n681)
74x882	1	32-bit lookahead carry generator		24	SN74AS882 (https://arc hive.org/details/bitsaver s_tidataBookVol3_25840 031/page/n683)
74x885	1	8-bit magnitude comparator		24	SN74AS885 (https://we b.archive.org/web/20170 403014245/http://www.ti. com/lit/ds/symlink/sn74 as885.pdf)
74x887	1	8-bit processor element (non- cascadable version of 74x888)		(68)	SN74AS887 (https://arc hive.org/details/bitsaver s_tidataBook_28346484/ 1986_LSI_Logic/page/n2 77)
74x888	1	8-bit processor slice		64	SN74AS888 (https://arc hive.org/details/bitsaver s_tidataBook_28346484/ 1986_LSI_Logic/page/n3 25)
74x889	1	8-bit processor slice		(68)	SN74AS889 (https://arc hive.org/details/bitsaver s_tidataBookuitsDataBo ok_32771470/page/n63 7)

74x890	1	microoperation sequencer			64	SN74AS890 (https://arc hive.org/details/bitsaver s_tidataBook_28346484/ page/n375)
74x891	1	microoperation sequencer			(68)	SN74AS891 (https://arc hive.org/details/bitsaver s_tidataBookuitsDataBo ok_32771470/page/n68 5)
74x895	1	8-bit memory address generator			(68)	SN74AS895 (https://arc hive.org/details/bitsaver s_tidataBook_28346484/ page/n393)
74x897	1	16-bit parallel/serial barrel shifter			(68)	SN74AS897A (https://ar chive.org/details/bitsave rs_tidataBook_2834648 4/page/n443)
74x899	1	9-bit latchable transceiver with parity generator / checker		three- state	(28)	74AC899 (https://archiv e.org/details/bitsavers_n ationaldaFACTDatabook _39311242/page/n431)
Part number	Units	Description	Input	Output	Pins	Datasheet
74x900	4	quad 2-input NAND gate		driver	14	SN74ALS900 (https://da tasheet.datasheetarchiv e.com/originals/distribut ors/Datasheets-112/DSA P0051456.pdf)
74x901	6	hex inverting TTL buffer			14	MM74C901 (https://archi ve.org/details/bitsavers_ nationaldaCMOSIntegrat edCircuits_16413029/pa ge/n93)
74C902	6	hex non-inverting TTL buffer			14	MM74C902 (https://archi ve.org/details/bitsavers_ nationaldaCMOSIntegrat edCircuits_16413029/pa ge/n93)
74ALS902	4	quad 2-input NOR gate		driver	14	SN74ALS902 (https://da tasheet.datasheetarchiv e.com/originals/distribut ors/Datasheets-111/DSA P0036721.pdf)
74C903	6	hex inverting PMOS buffer			14	MM74C903 (https://archi ve.org/details/bitsavers_ nationaldaCMOSIntegrat edCircuits_16413029/pa ge/n93)
74ALS903	4	quad 2-input NAND gate		open- collector driver	14	SN74ALS903 (https://da tasheet.datasheetarchiv e.com/originals/distribut ors/Datasheets-111/DSA P0036722.pdf)
74x904	6	hex non-inverting PMOS buffer			14	MM74C904 (https://archive.org/details/bitsavers_ nationaldaCMOSIntegrat

						edCircuits_16413029/pa ge/n93)
74x905	1	12-bit successive approximation register			24	MM74C905 (https://archi ve.org/details/bitsavers_ nationaldaCMOSIntegrat edCircuits_16413029/pa ge/n97)
74x906	6	hex open drain n-channel buffers		open- collector	14	MM74C906 (https://archi ve.org/details/bitsavers_ nationaldaCMOSIntegrat edCircuits_16413029/pa ge/n103)
74x907	6	hex open drain p-channel buffers			14	MM74C907 (https://archi ve.org/details/bitsavers_ nationaldaCMOSIntegrat edCircuits_16413029/pa ge/n103)
74x908	2	dual 2-input NAND 30 V / 250 mA relay driver			8	MM74C908 (https://archi ve.org/details/bitsavers_ nationaldaCMOSIntegrat edCircuits_16413029/pa ge/n105)
74x909	4	quad voltage comparator	analog	open- collector	14	MM74C909 (https://archi ve.org/details/bitsavers_ nationaldaCMOSIntegrat edCircuits_16413029/pa ge/n109)
74x910	1	256-bit RAM (64x4)		three- state	18	MM74C910 (https://archi ve.org/details/bitsavers_ nationaldaCMOSIntegrat edCircuits_16413029/pa ge/n115)
74x911	1	4-digit expandable display controller		three- state	28	MM74C911 (https://archi ve.org/details/bitsavers_ nationaldaCMOSDatabo ok_23595721/page/n13 5)
74x912	1	6-digit BCD display controller and driver		three- state	28	MM74C912 (https://archi ve.org/details/bitsavers_ nationaldaCMOSDatabo ok_23595721/page/n13 5)
74x913	1	6-digit BCD display controller and driver, no decimal point			24	MM74C913 (https://archi ve.org/details/bitsavers_ nationaldaCMOSDatabo ok_23595721/page/n13 5)
74x914	6	hex inverter gate, extended input voltage	Schmitt trigger		14	MM74C914 (https://archive.org/details/bitsavers_ nationaldaCMOSIntegrat edCircuits_16413029/pa ge/n117)
74x915	1	7-segment to BCD converter		three- state	18	MM74C915 (https://archi ve.org/details/bitsavers_ nationaldaCMOSDatabo ok_23595721/page/n14 1)

74x917	1	6-digit hex display controller and driver	three- state	28	MM74C917 (https://archi ve.org/details/bitsavers_ nationaldaLogicDataboo kVolume1_95500749/pa ge/n1333)
74x918	2	dual 2-input NAND 30 V / 250 mA relay driver		14	MM74C918 (https://archi ve.org/details/bitsavers_ nationaldaCMOSIntegrat edCircuits_16413029/pa ge/n105)
74x920	1	1024-bit RAM (256x4), separate data inputs and outputs	three- state	22	MM74C920 (https://archi ve.org/details/bitsavers_ nationaldaCMOSDatabo ok_23595721/page/n14 5)
74x921	1	1024-bit RAM (256x4)	three- state	18	MM74C921 (https://archi ve.org/details/bitsavers_ nationaldaCMOSDatabo ok_23595721/page/n14 5)
74x922	1	16-key encoder	three- state	18	MM74C922 (https://archi ve.org/details/bitsavers_ nationaldaCMOSDatabo ok_23595721/page/n14 9)
74x923	1	20-key encoder	three- state	20	MM74C923 (https://archi ve.org/details/bitsavers_ nationaldaCMOSDatabo ok_23595721/page/n14 9)
74x925	1	4-digit counter/display driver		16	MM74C925 (https://archi ve.org/details/bitsavers_ nationaldaCMOSDatabo ok_23595721/page/n15 5)
74x926	1	4-digit decade counter/display driver, carry out and latch (up to 9999)		16	MM74C926 (https://archi ve.org/details/bitsavers_ nationaldaCMOSDatabo ok_23595721/page/n15 5)
74x927	1	4-digit timer counter/display driver (up to 9599, intended as time elapsed, i.e. 9:59.9 min)		16	MM74C927 (https://archi ve.org/details/bitsavers_ nationaldaCMOSDatabo ok_23595721/page/n15 5)
74x928	1	4-digit counter/display driver (up to 1999)		16	MM74C928 (https://archi ve.org/details/bitsavers_ nationaldaCMOSDatabo ok_23595721/page/n15 5)
74x929	1	1024-bit RAM (1024x1), single chip select	three- state	16	MM74C929 (https://archi ve.org/details/bitsavers_ nationaldaCMOSDatabo ok_23595721/page/n15 5)
74x930	1	1024-bit RAM (1024x1), three chip selects	three- state	18	MM74C930 (https://archive.org/details/bitsavers_

						nationaldaCMOSDatabo ok_23595721/page/n15 5)
74x932	1	phase comparator			8	MM74C932 (https://archi ve.org/details/bitsavers_ nationaldaLogicDataboo kVolume1_95500749/pa ge/n1305)
74x933	1	7-bit address bus comparator			20	MM74C933 (https://archi ve.org/stream/NationalS emiconductor-CMOSDat abook1981#page/n5)
74934	1	ADC similar to ADC0829, see corresponding NSC datasheet				
74x935	1	ADC for 3.5-digit digital voltmeters, multiplexed 7- segment display outputs	analog		28	MM74C935 (https://archi ve.org/details/bitsavers_ nationaldaCMOSDatabo ok_23595721/page/n16 3)
74x936	1	ADC for 3.75-digit digital voltmeters, multiplexed 7-segment display outputs	analog		?	MM74C936 (https://archi ve.org/details/bitsavers_ nationaldaCMOSDatabo ok_23595721/page/n17 1)
74x937	1	ADC for 3.5-digit digital voltmeters, multiplexed BCD outputs	analog		24	MM74C937 (https://archi ve.org/details/bitsavers_ nationaldaDataAcquisitio nHandbook_38492992/p age/n83)
74x938	1	ADC for 3.75-digit digital voltmeters, multiplexed BCD outputs	analog		24	MM74C938 (https://archi ve.org/details/bitsavers_ nationaldaDataAcquisitio nHandbook_38492992/p age/n83)
74x940	1	octal bus/line drivers/line receivers	Schmitt trigger	three- state	20	DM74S940 (https://archi ve.org/stream/NationalS emiconductorLogicDatab ook1981/National%20Se miconductor%20Logic% 20Databook%201981#pa ge/n161)
74x941	1	octal bus/line drivers/line receivers	Schmitt trigger	three- state	20	DM74S941 (https://archi ve.org/stream/NationalS emiconductorLogicDatab ook1981/National%20Se miconductor%20Logic% 20Databook%201981#pa ge/n161)
74x942	1	300 baud Bell 103 modem (+/- 5 V supply)			20	MM74HC942 (https://arc hive.org/details/bitsaver s_nationaldaLogicDatab ookVolume1_95500749/ page/n639)
74x943	1	300 baud Bell 103 modem (single 5 V supply)			20	MM74HC943 (https://arc hive.org/details/bitsaver s_nationaldaLogicDatab
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						ookVolume1_95500749/ page/n645)
74x945	1	4-digit up/down counter, decoder and LCD driver, output latch			40	MM74C945 (https://archi ve.org/details/bitsavers_ nationaldaLogicDataboo kVolume1_95500749/pa ge/n1343)
74x946	1	4.5-digit counter, decoder and LCD driver, leading zero blanking			40	MM74C946 (https://archi ve.org/details/bitsavers_ nationaldaLogicDataboo kVolume1_95500749/pa ge/n1351)
74x947	1	4-digit up/down counter, decoder and LCD driver, leading zero blanking			40	MM74C947 (https://archi ve.org/details/bitsavers_ nationaldaLogicDataboo kVolume1_95500749/pa ge/n1343)
74x948	1	8-bit <u>ADC</u> with 16-channel analog multiplexer	analog	three- state	40	MM74C948 (https://archi ve.org/details/bitsavers_ nationaldaDataAcquisitio nHandbook_38492992/p age/n63)
74x949	1	8-bit <u>ADC</u> with 8-channel analog multiplexer	analog	three- state	28	MM74C949 (https://archi ve.org/details/bitsavers_ nationaldaCMOSDatabo ok_23595721/page/n17 3)
74x950	1	8-bit <u>ADC</u> with 8-channel analog multiplexer and sample and hold	analog	three- state	28	MM74C950 (https://archi ve.org/details/bitsavers_ nationaldaCMOSDatabo ok_23595721/page/n17 3)
74x952	1	dual rank 8-bit shift register, synchronous clear		three- state	18	DM74LS952 (https://arc hive.org/stream/National SemiconductorLogicDat abook1981/National%20 Semiconductor%20Logi c%20Databook%201981 #page/n417)
74C956	1	4-digit, 17-segment alpha- numeric LED display driver with memory and decoder			40	MM74C956 (https://archi ve.org/details/bitsavers_ nationaldaLogicDataboo kVolume1_95500749/pa ge/n1357)
74BCT956	1	octal bus transceiver and latch		three- state	24	SN74BCT956 (https://da tasheetspdf.com/pdf-file/ 1271601/Texas/SN74BC T956/1)
74x962	1	dual rank 8-bit shift register, register exchange mode		three- state	18	DM74LS962 (https://arc hive.org/stream/National SemiconductorLogicDat abook1981/National%20 Semiconductor%20Logi c%20Databook%201981 #page/n417)
74x963	1	dual rank 8-bit shift register, synchronous clear		three- state	20	SN74ALS963 (https://ar chive.org/details/bitsave

					rs_tidataBook_2834648 4/page/n461)
74x964	1	dual rank 8-bit shift register, synchronous and asynchronous clear	three- state	20	SN74ALS964 (https://ar chive.org/details/bitsave rs_tidataBook_2834648 4/page/n461)
74x968	1	controller/driver for 16k/64k/256k/1M dRAM		52	74F968 (https://archive. org/stream/NationalSemi conductor1988FASTAdv ancedSchottkyDataboo k/National%20Semicond uctor%201988%20FAS T%20Advanced%20Sch ottky%20Databook#pag e/n655)
74x978	1	octal flip-flop with serial scanner		24	74F978 (https://archive. org/stream/NationalSemi conductor1988FASTAdv ancedSchottkyDataboo k/National%20Semicond uctor%201988%20FAS T%20Advanced%20Sch ottky%20Databook#pag e/n667)
74x979	1	9-bit registered transceiver with parity generator/checker for <u>FutureBus</u>	three- state and open- collector	(48)	SN74BCT979 (https://ar chive.org/details/Texasl nstruments-TI-Data-Adv ancedLogicandBusInterf aceLogic1991OCR/page/ n447)
74x989	1	64-bit RAM (64x4), inverting output	three- state	16	MM74C989 (https://archi ve.org/details/bitsavers_ nationaldaLogicDataboo kVolume1_95500749/pa ge/n1313)
74x990	1	8-bit D-type transparent read- back latch, non-inverting	three- state	20	SN74ALS990 (http://ww w.ti.com/lit/gpn/sn74als9 90)
74x991	1	8-bit D-type transparent read- back latch, inverting	three- state	20	SN74ALS991 (https://ar chive.org/details/bitsave rs_tidataBook_2834648 4/page/n473)
74x992	1	9-bit D-type transparent read- back latch, non-inverting	three- state	24	SN74ALS992 (http://ww w.ti.com/lit/gpn/sn74als9 92)
74x993	1	9-bit D-type transparent read- back latch, inverting	three- state	24	SN74ALS993 (https://ar chive.org/details/bitsave rs_tidataBook_2834648 4/page/n481)
74x994	1	10-bit D-type transparent read-back latch, non- inverting	three- state	24	SN74ALS994 (https://ar chive.org/details/bitsave rs_tidataBook_2834648 4/page/n489)
74x995	1	10-bit D-type transparent read-back latch, inverting	three- state	24	SN74ALS995 (https://ar chive.org/details/bitsave rs_tidataBook_2834648 4/page/n489)

74x996	1	8-bit D-type edge-triggered read-back latch		three- state	24	SN74ALS996 (http://ww w.ti.com/lit/gpn/sn74als9 96)
Part number	Units	Description	Input	Output	Pins	Datasheet
74x1000	4	quad 2-input NAND gate		driver	14	SN74AS1000A (http://w ww.ti.com/lit/gpn/sn54as 1000a)
74x1002	4	quad 2-input NOR gate		driver	14	SN74ALS1002A (http://w ww.ti.com/lit/gpn/sn54al s1002a)
74x1003	4	quad 2-input NAND gate		open- collector driver	14	SN74ALS1003A (https:// archive.org/details/bitsa vers_tidataBookVol3_25 840031/page/n701)
74x1004	6	hex inverting buffer		driver	14	SN74ALS1004 (http://w ww.ti.com/lit/gpn/sn74al s1004)
74x1005	6	hex inverting buffer		open- collector driver	14	SN74ALS1005 (http://w ww.ti.com/lit/gpn/sn74al s1005)
74x1008	4	quad 2-input AND gate		driver	14	SN74AS1008A (http://w ww.ti.com/lit/gpn/sn74as 1008a)
74ALS1010	3	triple 3-input NAND gate		driver	14	SN74ALS1010A (https:// web.archive.org/web/201 70225141918/http://ww w.ti.com/lit/ds/symlink/s n74als1010a.pdf)
74AC1010, 74ACT1010	1	16x16-bit multiplier/accumulator		three- state	64	74AC1010 (https://archiv e.org/details/bitsavers_f airchilddldFACTLogicDat aBook_27153725/page/n 457)
74x1011	3	triple 3-input AND gate		driver	14	SN74ALS1011A (https:// archive.org/details/bitsa vers_tidataBookVol3_25 840031/page/n715)
74F1016	16	16-bit Schottky diode R-C bus termination array			(20)	SN74F1016 (http://www.t i.com/lit/gpn/sn74f1016)
74AC1016, 74ACT1016	1	16x16-bit multiplier		three- state	64	74AC1016 (https://archiv e.org/details/bitsavers_f airchilddldFACTLogicDat aBook_27153725/page/n 467)
74x1017	1	16x16-bit parallel multiplier		three- state	64	74AC1017 (https://archiv e.org/details/bitsavers_f airchilddldFACTLogicDat aBook_27153725/page/n 479)
74x1018	18	18-bit Schottky diode R-C bus termination array			(24)	SN74F1018 (https://data sheet.datasheetarchive. com/originals/distributor s/Datasheets-36/DSA-70 6945.pdf)

74x1020	2	dual 4-input NAND gate	driver	14	SN74ALS1020A (https:// archive.org/details/bitsa vers_tidataBookVol3_25 840031/page/n717)
74x1032	4	quad 2-input OR gate	driver	14	SN74AS1032A (https://w eb.archive.org/web/2017 0221113739/http://www.t i.com/lit/ds/symlink/sn7 4as1032a.pdf)
74x1034	6	hex non-inverting buffer	driver	14	SN74ALS1034 (http://w ww.ti.com/lit/gpn/sn54al s1034)
74x1035	6	hex non-inverting buffer	open- collector driver	14	SN74ALS1035 (http://w ww.ti.com/lit/gpn/sn54al s1035)
74x1036	4	quad 2-input NOR gate	driver	14	SN74ALS1036 (https://a rchive.org/details/bitsav ers_tidataBookVol3_258 40031/page/n729)
74x1050	12	12-bit Schottky diode bus termination array, clamp to GND		16	SN74S1050 (http://www. ti.com/lit/gpn/sn74s105 0)
74x1051	12	12-bit Schottky diode bus termination array, clamp to GND/V _{CC}		16	$\frac{\text{SN74S1051 (http://www.}}{\text{ti.com/lit/gpn/sn74s105}}$
74x1052	16	16-bit Schottky diode bus termination array, clamp to GND		20	SN74S1052 (https://arch ive.org/details/TexasInst ruments-TI-Data-Advanc edLogicandBusInterface Logic1991OCR/page/n47 1)
74x1053	16	16-bit Schottky diode bus termination array, clamp to GND/V _{CC}		20	SN74S1053 (http://www. ti.com/lit/gpn/sn74s105 3)
74x1056	8	8-bit Schottky diode bus termination array, clamp to GND		(16)	SN74F1056 (http://www.t i.com/lit/gpn/sn74f1056)
74x1071	10	10-bit bus termination array with bus-hold function		(14)	SN74ACT1071 (http://w ww.ti.com/lit/gpn/sn74ac t1071)
74x1073	16	16-bit bus termination array with bus-hold function		(20)	SN74ACT1073 (http://w ww.ti.com/lit/gpn/sn74ac t1073)
74x1074	2	dual D negative edge triggered flip-flop, asynchronous preset and clear		14	74FR1074 (https://datas heet.datasheetarchive.c om/originals/distributors/ Datasheets-11/DSA-210 975.pdf)
74x1181	1	4-bit arithmetic logic unit		24	SN74AS1181 (https://ar chive.org/details/bitsave rs_tidataBook_2834648 4/page/n503)

74x1240	1	octal buffer / line driver, inverting (lower-power version of 74x240)		three- state	20	SN74ALS1240 (https://a rchive.org/details/bitsav ers_tidataBookVol3_258 40031/page/n731)
74x1241	1	octal buffer / line driver, non- inverting (lower-power version of 74x241)		three- state	20	SN74ALS1241 (https://a rchive.org/details/bitsav ers_tidataBookVol3_258 40031/page/n731)
74x1242	1	quad bus transceiver, inverting (lower-power version of 74x242)		three- state	14	SN74ALS1242 (https://a rchive.org/details/bitsav ers_tidataBookVol3_258 40031/page/n735)
74x1243	1	quad bus transceiver, non- inverting (lower-power version of 74x243)		three- state	14	SN74ALS1243 (https://a rchive.org/details/bitsav ers_tidataBookVol3_258 40031/page/n735)
74x1244	1	octal buffer / driver, non- inverting (lower-power version of 74x244)		three- state	20	SN74ALS1244 (https://a rchive.org/details/bitsav ers_tidataBookVol3_258 40031/page/n739)
74x1245	1	octal bus transceiver (lower- power version of 74x245)		three- state	20	SN74ALS1245A (http://w ww.ti.com/lit/gpn/sn74al s1245a)
74x1280	1	9-bit parity generator/checker with registered outputs		three- state	20	QS74FCT1280 (https://w eb.archive.org/web/2018 1117162114/https://4don line.ihs.com/images/Vip MasterIC/IC/QSEM/QS EMD004/QSEMD004-3- 71.pdf)
74x1284	1	parallel printer interface transceiver / buffer (IEEE 1284)			20	74HCT1284 (http://pdf.d atasheetcatalog.com/dat asheet/philips/74HCT12 84PW.pdf)
74x1394	1	2-bit GTLP transceiver with split LV-TTL port		three- state and open- collector	(16)	SN74GTLP1394 (https:// www.ti.com/lit/gpn/SN74 GTLP1394)
74x1395	2	Dual 1-bit GTLP transceiver with split LV-TTL port		three- state and open- collector	(20)	SN74GTLP1395 (https:// www.ti.com/lit/gpn/SN74 GTLP1395)
74x1403	1	8-bit bus receiver plus 4-bit bus driver	Schmitt trigger	three- state	(32)	74LVT1403 (https://data sheet.datasheetarchive. com/originals/distributor s/Datasheets-25/DSA-49 7532.pdf)
74x1404	1	oscillator driver	Schmitt trigger		(8)	SN74LVC1404 (http://ww w.ti.com/lit/gpn/sn74lvc1 404)
74x1604	1	dual 8-bit transparent latch with output multiplexer			28	74F1604 (https://cdn.dat asheetspdf.com/pdf-dow n/7/4/F/74F1604_Philips Semiconductors.pdf)

74x1612	1	18-bit LV-TTL-to-GTLP adjustable-edge-rate universal bus transceiver	three- state and open- collector	(64)	SN74GTLPH1612 (http s://e2e.ti.com/cfs-file/ key/communityserver-di scussions-components-f iles/151/SN74GTLPH16 12-Rev2005.pdf)
74ALS1616	1	16x16-bit multimode multiplier	three- state	64	SN74ALS1616 (https://a rchive.org/details/bitsav ers_icMaster19_159569 496/page/n919)
74GTLPH1616	1	17-bit LV-TTL-to-GTLP adjustable-edge-rate universal bus transceiver with buffered clock outputs	three- state and open- collector	(64)	SN74GTLPH1616 (http s://media.digikey.com/p df/Data%20Sheets/Texa s%20Instruments%20P DFs/sn74gtlph1616.pdf)
74x1620	1	octal bus transceiver, inverting	three- state	20	SN74ALS1620 (https://a rchive.org/details/bitsav ers_tidataBookVol3_258 40031/page/n747)
74x1621	1	octal bus transceiver, non- inverting	open- collector	20	SN74ALS1621 (https://a rchive.org/details/bitsav ers_tidataBookVol3_258 40031/page/n747)
74x1622	1	octal bus transceiver, inverting	open- collector	20	SN74ALS1622 (https://a rchive.org/details/bitsav ers_tidataBookVol3_258 40031/page/n747)
74x1623	1	octal bus transceiver, non- inverting	three- state	20	SN74ALS1623 (https://a rchive.org/details/bitsav ers_tidataBookVol3_258 40031/page/n747)
74x1627	1	18-bit LV-TTL-to-GTLP adjustable-edge-rate bus transceiver with source synchronous clock outputs	three- state and open- collector	(64)	SN74GTLPH1627 (http s://media.digikey.com/p df/Data%20Sheets/Texa s%20Instruments%20P DFs/sn74gtlph1627%5b 1%5d.pdf)
74x1631	1	quad bus driver with complementary outputs	three- state	16	SN74ALS1631 ^{[10]:3-336}
74x1638	1	octal bus transceiver, inverting (lower-power version of 74x638)	three- state and open- collector	20	SN74ALS1638 (https://a rchive.org/details/bitsav ers_tidataBookVol3_258 40031/page/n753)
74x1639	1	octal bus transceiver, non- inverting (lower-power version of 74x639)	three- state and open- collector	20	SN74ALS1639 (https://a rchive.org/details/bitsav ers_tidataBookVol3_258 40031/page/n753)
74x1640	1	octal bus transceiver, inverting (lower-power version of 74x640)	three- state	20	SN74ALS1640A (http://w ww.ti.com/lit/gpn/sn74al s1645a)
74x1641	1	octal bus transceiver, non- inverting (lower-power version of 74x641)	open- collector	20	SN74ALS641 (https://ar chive.org/details/bitsave rs_tidataBookVol3_2584 0031/page/n757)

74x1642	1	octal bus transceiver, inverting (lower-power version of 74x642)	open- collector	20	SN74ALS642 (https://ar chive.org/details/bitsave rs_tidataBookVol3_2584 0031/page/n757)
74x1643	1	octal bus transceiver, inverting and non-inverting (lower-power version of 74x643)	three- state	20	SN74ALS643 (https://ar chive.org/details/bitsave rs_tidataBookVol3_2584 0031/page/n757)
74x1644	1	octal bus transceiver, inverting and non-inverting (lower-power version of 74x644)	open- collector	20	SN74ALS644 (https://ar chive.org/details/bitsave rs_tidataBookVol3_2584 0031/page/n757)
74ALS1645	1	octal bus transceiver, non- inverting (lower-power version of 74x645)	three- state	20	SN74ALS1645A (http://w ww.ti.com/lit/gpn/sn74al s1645a)
74GTLPH1645	1	16-bit LV-TTL-to-GTLP adjustable-edge-rate bus transceiver	three- state and open- collector	(56)	SN74GTLPH1645 (http s://www.ti.com/lit/gpn/sn 74gtlph1645)
74x1650	2	dual 9-bit <u>Futurebus</u> universal storage transceiver with split TTL I/O	three- state and open- collector	(100)	SN74FB1650 (https://arc hive.org/details/bitsaver s_tidataBookiCMOSTec hnologyDataBook_40217 042/page/n689)
74x1651	2	9-bit and 8-bit Futurebus universal storage transceivers with delayed buffered clock with split TTL I/O	three- state and open- collector	(100)	SN74FB1651 (https://dat asheet.datasheetarchiv e.com/originals/distribut ors/Datasheets-36/DSA- 703111.pdf)
74x1653	2	9-bit and 8-bit Futurebus universal storage transceivers with delayed buffered clock with split 3.3V TTL I/O	three- state and open- collector	(100)	SN74FB1653 (http://ww w.ti.com/lit/gpn/SN74FB 1653)
74x1655	2	dual 8-bit GTL universal storage transceivers with live insertion	three- state and open- collector	(64)	SN74GTL1655 (http://w ww.ti.com/lit/gpn/SN74G TL1655)
74x1760	1	10-bit 4-way latched address multiplexer	three- state	64	74F1760 (https://datash eet.datasheetarchive.co m/originals/distributors/D atasheets-111/DSAP003 4403.pdf)
74x1761	1	dRAM and interrupt vector controller		48	74F1761 (https://archiv e.org/details/bitsavers_s igneticsdaManual_57966 640/page/n911)
74x1762	1	dRAM address controller		40	74F1762 (https://archiv e.org/details/bitsavers_s igneticsdaManual_57966 640/page/n913)
74x1763	1	single-port dRAM controller		48	74F1763 (https://archiv e.org/details/bitsavers_s

					igneticsdaManual_57966 640/page/n915)
74x1764	1	dual-port dRAM controller		48	74F1764 (https://archiv e.org/details/bitsavers_s igneticsdaManual_57966 640/page/n917)
74x1765	1	dual-port dRAM controller with address latch		48	74F1765 (https://archiv e.org/details/bitsavers_s igneticsdaManual_57966 640/page/n917)
74x1766	1	burst mode dRAM controller		48	74F1766 (https://datash eet.datasheetarchive.co m/originals/scans/Scans -054/DSAIH00097122.pd f)
74x1779	1	8-bit bidirectional binary counter	three- state	16	74F1779 (https://cdn.dat asheetspdf.com/pdf-dow n/7/4/F/74F1779_Philips Semiconductors.pdf)
74x1801	1	FM, MFM, and DM encoder / decoder, data rates up to 10 MHz		24	74LS1801 (https://datas heet.datasheetarchive.c om/originals/scans/Scan s-002/Scans-0052487.pd f)
74x1802	1	SerDes with ECC and CRC, data rates up to 10 MHz	three- state	48	74LS1802 (https://4donli ne.ihs.com/images/VipM asterIC/IC/SIGC/SIGCD 005/SIGCD005-7-26.pdf)
74x1803	1	quad clock driver		14	MC74F1803 (https://arch ive.org/details/bitsavers _motoroladaFASTandLS TTLData_35934218/pag e/n309)
74x1804	6	hex 2-input NAND	driver	20	DM74AS1804 (https://ar chive.org/details/bitsave rs_nationaldaicDatabook _22808448/page/n639)
74x1805	6	hex 2-input NOR	driver	20	DM74AS1805 (https://ar chive.org/details/bitsave rs_nationaldaicDatabook _22808448/page/n641)
74x1808	6	hex 2-input AND	driver	20	DM74AS1808 (https://ar chive.org/details/bitsave rs_nationaldaicDatabook _22808448/page/n643)
74x1811	1	FM, MFM, and DM encoder / decoder, data rates up to 20 MHz		24	74LS1811 (https://4donli ne.ihs.com/images/VipM asterIC/IC/SIGC/SIGCD 005/SIGCD005-7-36.pdf)
74x1812	1	SerDes with ECC and CRC, data rates up to 30 MHz	three- state	48	74LS1812 (https://4donli ne.ihs.com/images/VipM asterIC/IC/SIGC/SIGCD 005/SIGCD005-7-37.pdf)
74x1821	1	10-bit bus interface flip-flops	three- state	24	SN74AS1821 (http://www.elektronikjk.pl/element

						y_czynne/IC/SN74AS18 21.pdf)
74x1823	1	9-bit bus interface flip-flops with clear		three- state	24	SN74AS1823 (https://da tasheet.datasheetarchiv e.com/originals/scans/S cans-067/DSA2IH00218 035.pdf)
74x1832	6	hex 2-input OR		driver	20	DM74ALS1832 (https://a rchive.org/details/bitsav ers_nationaldaicDataboo k_22808448/page/n645)
74x1841	1	10-bit bus interface transparent latches		three- state	24	SN74AS1841 (https://da tasheet.datasheetarchiv e.com/originals/scans/S cans-067/DSA2IH00218 036.pdf)
74x1843	1	9-bit bus interface transparent latches with clear		three- state	24	SN74AS1843 (https://da tasheet.datasheetarchiv e.com/originals/distribut ors/Datasheets-36/DSA- 706295.pdf)
Part number	Units	Description	Input	Output	Pins	Datasheet
74x2000	1	direction discriminator with microprocessor interface		three- state	28	SN74LS2000 (https://dat asheet.datasheetarchiv e.com/originals/scans/S cans-110/22.pdf)
74x2003	1	8-bit level translator			(20)	SN74GTL2003 (http://w ww.ti.com/lit/gpn/SN74G TL2003)
74x2006	1	13-bit GTL to 3.3V TTL level translator		open- collector	(28)	SN74GTL2006 (http://w ww.ti.com/lit/gpn/SN74G TL2006)
74x2007	1	12-bit GTL to 3.3V TTL level translator		open- collector	(28)	SN74GTL2007 (http://w ww.ti.com/lit/gpn/SN74G TL2007)
74x2010	1	10-bit level translator			(24)	SN74GTL2010 (http://w ww.ti.com/lit/gpn/SN74G TL2010)
74x2014	1	4-bit <u>GTL</u> to TTL transceiver		three- state and open- collector	(14)	SN74GTL2014 (http://w ww.ti.com/lit/gpn/SN74G TL2014)
74x2031	1	9-bit <u>Futurebus</u> address/data transceiver		three- state and open- collector	(48)	SN74FB2031 (https://arc hive.org/details/bitsaver s_tidataBookiCMOSTec hnologyDataBook_40217 042/page/n695)
74x2032	1	9-bit Futurebus competition transceiver		three- state and open- collector	(48)	SN74FB2032 (https://arc hive.org/details/bitsaver s_tidataBookiCMOSTec hnologyDataBook_40217 042/page/n701)
74FB2033	1	8-bit Futurebus registered transceiver with split TTL I/O		three- state and	(52)	SN74FB2033 (https://arc hive.org/details/bitsaver s_tidataBookiCMOSTec
			open- collector		hnologyDataBook_40217 042/page/n709)	
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74GTLP2033	1	8-bit GTLP registered transceiver with split LV-TTL I/O	three- state and open- collector	(48)	SN74GTLP2033 (https:// www.ti.com/lit/gpn/SN74 GTLP2033)	
74x2034	1	8-bit <u>GTLP</u> adjustable-edge- rate registered transceiver with split LV-TTL I/O	three- state and open- collector	(48)	SN74GTLP2034 (https:// media.digikey.com/pdf/D ata%20Sheets/Texas%2 OInstruments%20PDFs/ sn74gtlp2034%5b1%5d. pdf)	
74x2040	1	8-bit <u>Futurebus</u> transceiver with split TTL I/O	three- state and open- collector	(48)	SN74FB2040 (https://arc hive.org/details/bitsaver s_tidataBookiCMOSTec hnologyDataBook_40217 042/page/n719)	
74x2041	1	7-bit <u>Futurebus</u> transceiver with split TTL I/O	three- state and open- collector	(52)	SN74FB2041 (https://arc hive.org/details/bitsaver s_tidataBookiCMOSTec hnologyDataBook_40217 042/page/n725)	
74x2107	1	12-bit GTL to 3.3V TTL level translator	open- collector	(28)	SN74GTL2107 (http://w ww.ti.com/lit/gpn/SN74G TL2107)	
74x2125	4	quad bus buffer	three- state, 25 Ω series resistor	(14)	TC74VCX2125 (https://d atasheet.datasheetarchi ve.com/originals/distribu tors/Datasheets-2/DSA- 33230.pdf)	
74x2140	1	8k x 18 cache data RAM	three- state	(52)	SN74ACT2140A (https:// usermanual.wiki/Docum ent/1990TICacheMemor yManagementDataBook. 1210032352.pdf)	
74x2150	1	512 x 8 cache address comparator		24	SN74ACT2150A (https:// usermanual.wiki/Docum ent/1990TICacheMemor yManagementDataBook. 1210032352.pdf)	
74ACT2151	1	1k x 11 cache address comparator		28	SN74ACT2151 (https://u sermanual.wiki/Docume nt/1990TICacheMemory ManagementDataBook.1 210032352.pdf)	
74FCT2151	1	8-line to 1-line multiplexer	25 Ω series resistor	(16)	CD74FCT2151 (https://a rchive.org/details/bitsav ers_harrisdataCTLogic_2 5505286/page/n187)	
74x2152	1	2k x 8 cache address comparator		28	SN74ACT2152A (https:// usermanual.wiki/Docum ent/1990TICacheMemor yManagementDataBook. 1210032352.pdf)	
74ACT2153	1	1k x 11 cache address comparator	open- collector	28	SN74ACT2153 (https://u sermanual.wiki/Docume	

					nt/1990TICacheMemory ManagementDataBook.1 210032352.pdf)
74FCT2153	2	dual 4-line to 1-line multiplexer	25 Ω series resistor	(16)	CD74FCT2153 (https://a rchive.org/details/bitsav ers_harrisdataCTLogic_2 5505286/page/n191)
74x2154	1	2k x 8 cache address comparator	open- collector	28	SN74ACT2154A (https:// usermanual.wiki/Docum ent/1990TICacheMemor yManagementDataBook. 1210032352.pdf)
74x2155	1	2k x 8 burst cache address comparator	three- state	(44)	SN74ACT2155 (https://u sermanual.wiki/Docume nt/1990TICacheMemory ManagementDataBook.1 210032352.pdf)
74x2156	1	16k x 4 burst cache address comparator	three- state	(44)	SN74ACT2156 (https://u sermanual.wiki/Docume nt/1990TICacheMemory ManagementDataBook.1 210032352.pdf)
74ACT2157	1	2k x 16 cache address comparator	three- state	(44)	SN74ACT2157 (https://u sermanual.wiki/Docume nt/1990TICacheMemory ManagementDataBook.1 210032352.pdf)
74FCT2157	4	quad 2-line to 1-line multiplexer	25 Ω series resistor	(16)	CD74FCT2157 (https://a rchive.org/details/bitsav ers_harrisdataCTLogic_2 5505286/page/n197)
74x2158	1	8k x 9 cache address comparator	three- state	(44)	SN74ACT2158 (https://u sermanual.wiki/Docume nt/1990TICacheMemory ManagementDataBook.1 210032352.pdf)
74x2159	1	8k x 9 cache address comparator	three- state	(44)	SN74ACT2159 (https://u sermanual.wiki/Docume nt/1990TICacheMemory ManagementDataBook.1 210032352.pdf)
74x2160	1	8k x 4 2-way cache address comparator	three- state	(32)	SN74ACT2160 (https://u sermanual.wiki/Docume nt/1990TICacheMemory ManagementDataBook.1 210032352.pdf)
74x2161	1	synchronous presettable 4- bit binary counter, asynchronous clear	25 Ω series resistor	16	QS74FCT2161T (https:// archive.org/details/Qualit ySemiconductor-1991Da tabookOCR/page/n313)
74ACT2163, 74BCT2163	1	16k x 5 cache address comparator	three- state	(32)	SN74ACT2163 (https://u sermanual.wiki/Docume nt/1990TICacheMemory ManagementDataBook.1 210032352.pdf)
74FCT2163	1	synchronous presettable 4- bit binary counter,	25 Ω series	16	QS74FCT2163T (https:// archive.org/details/Qualit

		synchronous clear	resistor		ySemiconductor-1991Da tabookOCR/page/n313)
74x2164	1	16k x 5 cache address comparator	three- state	(32)	SN74ACT2164 (https://u sermanual.wiki/Docume nt/1990TICacheMemory ManagementDataBook.1 210032352.pdf)
74x2166	1	16k x 5 cache address comparator with input latches	three- state	(32)	SN74BCT2166 (https://u sermanual.wiki/Docume nt/1990TICacheMemory ManagementDataBook.1 210032352.pdf)
74x2191	1	synchronous presettable 4- bit binary up/down counter, common clock	25 Ω series resistor	16	QS74FCT2191T (https:// archive.org/details/Qualit ySemiconductor-1991Da tabookOCR/page/n321)
74x2193	1	synchronous presettable 4- bit binary counter, separate up/down clocks	25 Ω series resistor	16	QS74FCT2193T (https:// archive.org/details/Qualit ySemiconductor-1991Da tabookOCR/page/n329)
74x2226	2	dual 64-bit FIFO memories (64x1)		(24)	SN74ACT2226 (http://w ww.ti.com/lit/gpn/sn74ac t2226)
74x2227	2	dual 64-bit FIFO memories (64x1)	three- state	(28)	SN74ACT2227 (http://w ww.ti.com/lit/gpn/sn74ac t2227)
74x2228	2	dual 256-bit FIFO memories (256x1)		(24)	SN74ACT2228 (http://w ww.ti.com/lit/gpn/sn74ac t2226)
74x2229	2	dual 256-bit FIFO memories (256x1)	three- state	(28)	SN74ACT2229 (http://w ww.ti.com/lit/gpn/sn74ac t2227)
74x2232	1	512-bit FIFO memory (64x8)	three- state	24	SN74ALS2232A (https:// archive.org/details/bitsa vers_tidataBookeFIFOM emoriesDatabook_63352 841/page/n167)
74x2233	1	576-bit FIFO memory (64x9)	three- state	28	SN74ALS2233A (https:// archive.org/details/bitsa vers_tidataBookeFIFOM emoriesDatabook_63352 841/page/n175)
74x2235	1	18432-bit bidirectional FIFO memory (2x1024x9)	three- state	(44)	SN74ACT2235 (https://a rchive.org/details/bitsav ers_tidataBookeFIFOMe moriesDatabook_633528 41/page/n203)
74x2236	1	18432-bit bidirectional FIFO memory (2x1024x9)	three- state	(44)	SN74ACT2236 (https://a rchive.org/details/bitsav ers_tidataBookeFIFOMe moriesDatabook_633528 41/page/n215)
74x2238	1	576-bit bidirectional FIFO memory (2x32x9)	three- state	40	SN74ALS2238 (https://a rchive.org/details/bitsav ers_tidataBookeFIFOMe

						moriesDatabook_633528 41/page/n157)
74x2240	2	dual 4-bit bidirectional buffer / line driver, inverting		three- state, 25 Ω series resistor	20	SN74BCT2240 (https://a rchive.org/details/bitsav ers_tidataBookerfaceLog icDataBook_4501982/pa ge/n81)
74x2241	2	dual 4-bit bidirectional buffer / line driver, non-inverting		three- state, 25 Ω series resistor	20	SN74BCT2241 (https://a rchive.org/details/bitsav ers_tidataBookerfaceLog icDataBook_4501982/pa ge/n85)
74x2242	1	4-bit bus transceiver, inverting		three- state, 25 Ω series resistor	14	SN74ALS2242 (https://a rchive.org/details/bitsav ers_tidataBooktaBook_6 0160366/page/n951)
74x2243	1	4-bit bus transceiver, non- inverting		three- state, 25 Ω series resistor	(14)	74F2243 (https://datash eet.datasheetarchive.co m/originals/distributors/D atasheets-11/DSA-2097 24.pdf)
74x2244	2	dual 4-bit buffer / line driver, non-inverting		three- state, 25 Ω series resistor	20	SN74BCT2244 (https://a rchive.org/details/bitsav ers_tidataBookerfaceLog icDataBook_4501982/pa ge/n89)
74x2245	1	octal bus transceiver		three- state, 25 Ω series resistor	20	SN74ABT2245 (https://a rchive.org/details/bitsav ers_tidataBookiCMOSTe chnologyDataBook_4021 7042/page/n599)
74x2253	2	dual 4-line to 1-line multiplexer		three- state, 25 Ω series resistor	(16)	CD74FCT2253 (https://a rchive.org/details/bitsav ers_harrisdataCTLogic_2 5505286/page/n191)
74x2257	4	quad 2-line to 1-line multiplexer		three- state, 25 Ω series resistor	(16)	CD74FCT2257 (https://a rchive.org/details/bitsav ers_harrisdataCTLogic_2 5505286/page/n197)
74x2273	8	octal D-type flip-flop with common clock and reset		25 Ω series resistor	(20)	CD74FCT2273 (https://a rchive.org/details/bitsav ers_harrisdataCTLogic_2 5505286/page/n215)
74x2299	1	8-bit universal shift register		three- state, 25 Ω series resistor	20	QS74FCT2299T (https:// archive.org/details/Qualit ySemiconductor-1991Da tabookOCR/page/n363)
74x2323	2	dual line receiver	analog		(8)	SN74LS2323 (http://ww w.ti.com/lit/gpn/sn74ls23 23)
74x2373	1	8-bit transparent latch		three- state, 25 Ω	(20)	CD74FCT2373 (https://a rchive.org/details/bitsav

				series resistor		ers_harrisdataCTLogic_2 5505286/page/n219)
74x2374	8	octal D-type flip-flop with common clock		three- state, 25 Ω series resistor	(20)	CD74FCT2374 (https://a rchive.org/details/bitsav ers_harrisdataCTLogic_2 5505286/page/n227)
74x2377	1	8-bit register with clock enable		25 Ω series resistor	20	QS74FCT2377T (https:// archive.org/details/Qualit ySemiconductor-1991Da tabookOCR/page/n381)
74x2400	2	dual 4-bit buffer, inverting	Schmitt trigger	three- state	20	74THC2400 (http://www.i c72.com/pdf_file/i/18945 1.pdf)
74x2410	1	11-bit MOS memory driver, non-inverting		three- state, 25 Ω series resistor	28	SN74BCT2410 (https://a rchive.org/details/TexasI nstruments-TI-Data-Adv ancedLogicandBusInterf aceLogic1991OCR/page/ n747)
74x2411	1	11-bit MOS memory driver, inverting		three- state, 25 Ω series resistor	28	SN74BCT2411 (https://a rchive.org/details/Texasl nstruments-TI-Data-Adv ancedLogicandBusInterf aceLogic1991OCR/page/ n749)
74x2414	2	dual 2-to-4 line decoder with supply voltage monitor			20	SN74BCT2414 (https://d atasheet.datasheetarchi ve.com/originals/distribu tors/Datasheets-17/DSA -337707.pdf)
74x2420	1	16-bit <u>NuBus</u> address/data transceiver and register		three- state	(68)	SN74BCT2420 (https://a rchive.org/details/bitsav ers_tidataBookProducts _10042209/page/n29)
74x2423	1	16-bit latched multiplexer/demultiplexer <u>NuBus</u> transceiver, inverting		three- state	(68)	SN74BCT2423 (https://a rchive.org/details/bitsav ers_tidataBookProducts _10042209/page/n39)
74x2424	1	16-bit latched multiplexer/demultiplexer <u>NuBus</u> transceiver, non- inverting		three- state	(68)	SN74BCT2424 (https://a rchive.org/details/bitsav ers_tidataBookProducts _10042209/page/n39)
74x2425	1	Macintosh Coprocessor Platform NuBus address/data registered transceiver		three- state	(100)	SN74BCT2425 (https://a rchive.org/details/bitsav ers_tidataBookProducts _10042209/page/n49)
74x2440	1	NuBus interface controller			(68)	SN74ACT2440 (https://a rchive.org/details/bitsav ers_tidataBookProducts _10042209/page/n61)
74x2441	1	NuBus interface controller			(100)	SN74ACT2441 (https://a rchive.org/details/bitsav ers_tidataBookProducts _10042209/page/n93)

74x2442	1	NuBus block slave address generator	three- state	(20)	SN74ALS2442 (https://a rchive.org/details/bitsav ers_tidataBookProducts _10042209/page/n145)
74x2509	1	9-output clock driver with PLL	three- state	(24)	HD74CDC2509 (https://d atasheet.datasheetarchi ve.com/originals/distribu tors/Datasheets-13/DSA -248016.pdf)
74x2510	1	10-output clock driver with PLL	three- state	(24)	HD74CDC2510 (https://d atasheet.datasheetarchi ve.com/originals/distribu tors/Datasheets-13/DSA -248017.pdf)
74x2525	1	8-output clock driver		14	74AC2525 (https://archiv e.org/details/bitsavers_n ationaldaFACTDatabook _39311242/page/n443)
74x2526	1	8-output clock driver with input multiplexer		16	74AC2526 (https://archiv e.org/details/bitsavers_n ationaldaFACTDatabook _39311242/page/n443)
74x2533	1	8-bit bus interface latch, inverting	three- state, 25 Ω series resistor	20	QS74FCT2533T (https:// archive.org/details/Qualit ySemiconductor-1991Da tabookOCR/page/n369)
74x2534	1	8-bit bus interface register, inverting	three- state, 25 Ω series resistor	20	QS74FCT2534T (https:// archive.org/details/Qualit ySemiconductor-1991Da tabookOCR/page/n375)
74x2540	1	8-bit buffer / line driver, inverting	three- state, 25 Ω series resistor	20	SN74ALS2540 (https://a rchive.org/details/bitsav ers_tidataBooktaBook_6 0160366/page/n955)
74x2541	1	8-bit buffer / line driver, non- inverting	three- state, 25 Ω series resistor	20	SN74ALS2541 (https://a rchive.org/details/bitsav ers_tidataBooktaBook_6 0160366/page/n955)
74x2543	1	8-bit latched transceiver, non-inverting	three- state, 25 Ω series resistor	24	QS74FCT2543T (https:// archive.org/details/Qualit ySemiconductor-1991Da tabookOCR/page/n399)
74x2544	1	8-bit latched transceiver, inverting	three- state, 25 Ω series resistor	24	QS74FCT2544T (https:// archive.org/details/Qualit ySemiconductor-1991Da tabookOCR/page/n399)
74x2573	1	8-bit transparent latch	three- state, 25 Ω series resistor	20	QS74FCT2573T (https:// archive.org/details/Qualit ySemiconductor-1991Da tabookOCR/page/n407)

	74x2574	8	octal D-type flip-flop with common clock	three- state, 25 Ω series resistor	20	QS74FCT2574T (https:// archive.org/details/Qualit ySemiconductor-1991Da tabookOCR/page/n413)
-	74x2620	1	octal bus transceiver / MOS driver, inverting	three- state, 25 Ω series resistor	20	SN74AS2620 (https://ar chive.org/details/bitsave rs_tidataBookVol3_2584 0031/page/n763)
	74x2623	1	octal bus transceiver / MOS driver, non-inverting	three- state, 25 Ω series resistor	20	SN74AS2623 (https://ar chive.org/details/bitsave rs_tidataBookVol3_2584 0031/page/n763)
	74x2640	1	octal bus transceiver / MOS driver, inverting	three- state, 25 Ω series resistor	20	SN74AS2640 (https://ar chive.org/details/bitsave rs_tidataBookVol3_2584 0031/page/n767)
	74x2643	1	octal bus transceiver, mix of inverting and non-inverting outputs	three- state, 25 Ω series resistor	20	74F2643 (https://datash eet.datasheetarchive.co m/originals/distributors/D atasheets-22/DSA-4257 42.pdf)
	74x2645	1	octal bus transceiver / MOS driver, non-inverting	three- state, 25 Ω series resistor	20	SN74AS2645 (https://ar chive.org/details/bitsave rs_tidataBookVol3_2584 0031/page/n767)
	74x2646	1	octal registered transceiver, non-inverting	three- state, 25 Ω series resistor	24	QS74FCT2646T (https:// archive.org/details/Qualit ySemiconductor-1991Da tabookOCR/page/n419)
-	74x2648	1	octal registered transceiver, inverting	three- state, 25 Ω series resistor	24	QS74FCT2648T (https:// archive.org/details/Qualit ySemiconductor-1991Da tabookOCR/page/n419)
-	74x2651	1	octal registered transceiver, inverting	three- state, 25 Ω series resistor	24	QS74FCT2651T (https:// archive.org/details/Qualit ySemiconductor-1991Da tabookOCR/page/n427)
	74x2652	1	octal registered transceiver, non-inverting	three- state, 25 Ω series resistor	24	QS74FCT2652T (https:// archive.org/details/Qualit ySemiconductor-1991Da tabookOCR/page/n427)
	74S2708	1	8192-bit PROM (1024x8)	three- state	24	SN74S2708 (https://arch ive.org/details/bitsavers _tidataBookcomputerCo mponentsDataBook_168 51665/page/n177)
	74AC2708	1	576-bit FIFO memory (64x9)	three- state	28	74AC2708 (https://archiv e.org/details/bitsavers_n

					ationaldaFACTDatabook _39311242/page/n445)
74x2725	1	4608-bit FIFO memory (512x9)		28	74ACT2725 (https://arch ive.org/details/bitsavers nationaldaFACTDatabo ok_39311242/page/n46 1)
74x2726	1	4608-bit bidirectional FIFO memory (512x9)		28	74ACT2726 (https://arch ive.org/details/bitsavers nationaldaFACTDatabo ok_39311242/page/n46 1)
74x2821	1	10-bit D-type flip-flop	three- state, 25 Ω series resistor	24	QS74FCT2821T (https:// archive.org/details/Qualit ySemiconductor-1991Da tabookOCR/page/n435)
74x2823	1	9-bit D-type flip-flop with clear	three- state, 25 Ω series resistor	24	QS74FCT2823T (https:// archive.org/details/Qualit ySemiconductor-1991Da tabookOCR/page/n435)
74x2825	1	8-bit D-type flip-flop with clear and clock enable	three- state, 25 Ω series resistor	24	QS74FCT2825T (https:// archive.org/details/Qualit ySemiconductor-1991Da tabookOCR/page/n435)
74x2827	1	10-bit buffer, non-inverting	three- state, 25 Ω series resistor	24	SN74BCT2827A (https:// archive.org/details/bitsa vers_tidataBookerfaceLo gicDataBook_4501982/p age/n93)
74x2828	1	10-bit buffer, inverting	three- state, 25 Ω series resistor	24	SN74BCT2828A (https:// archive.org/details/bitsa vers_tidataBookerfaceLo gicDataBook_4501982/p age/n93)
74x2833	1	8-bit bus transceiver with parity error flip-flop	three- state, 25 Ω series resistor	24	QS74FCT2833T (https:// archive.org/details/Qualit ySemiconductor-1991Da tabookOCR/page/n451)
74x2841	1	10-bit transparent latch	three- state, 25 Ω series resistor	24	QS74FCT2841T (https:// archive.org/details/Qualit ySemiconductor-1991Da tabookOCR/page/n453)
74x2843	1	9-bit transparent latch with asynchronous reset	three- state, 25 Ω series resistor	24	QS74FCT2843T (https:// archive.org/details/Qualit ySemiconductor-1991Da tabookOCR/page/n453)
74x2845	1	8-bit transparent latch with asynchronous reset and multiple output enable	three- state, 25 Ω series resistor	24	QS74FCT2845T (https:// archive.org/details/Qualit ySemiconductor-1991Da tabookOCR/page/n453)

74x2853	1	8-bit bus transceiver with parity error latch	three- state, 25 Ω series resistor	24	QS74FCT2853T (https:// archive.org/details/Qualit ySemiconductor-1991Da tabookOCR/page/n451)
74x2861	1	10-bit non-inverting bus transceiver	three- state, 25 Ω series resistor	24	QS74FCT2861T (https:// archive.org/details/Qualit ySemiconductor-1991Da tabookOCR/page/n463)
74x2862	1	10-bit inverting bus transceiver	three- state, 25 Ω series resistor	24	QS74FCT2862T (https:// archive.org/details/Qualit ySemiconductor-1991Da tabookOCR/page/n463)
74x2863	1	9-bit non-inverting bus transceiver with dual output enable	three- state, 25 Ω series resistor	24	QS74FCT2863T (https:// archive.org/details/Qualit ySemiconductor-1991Da tabookOCR/page/n463)
74x2864	1	9-bit inverting bus transceiver with dual output enable	three- state, 25 Ω series resistor	24	QS74FCT2864T (https:// archive.org/details/Qualit ySemiconductor-1991Da tabookOCR/page/n463)
74x2952	1	octal bus transceiver and register, non-inverting	three- state	24	SN74LVC2952A (https:// archive.org/stream/Texa sInstrumentsLVCAndLV DataBook1998/Texas_In struments_LVC_and_LV _Data_Book_1998#pag e/n391)
74x2953	1	octal bus transceiver and register, inverting	three- state	24	74F2953 (https://archiv e.org/details/bitsavers_s igneticsdaManual_57966 640/page/n945)
74x2960	1	error detection and correction (EDAC), equivalent to Am2960	three- state	48	MC74F2960 (https://arch ive.org/details/bitsavers _motoroladaSchottkyTT LData_33878952/page/n 629)
74x2961	1	4-bit EDAC bus buffer, inverting, equivalent to Am2961	three- state	24	MC74F2961A (https://da tasheetspdf.com/pdf-file/ 501240/Motorola/MC74F 2961A/1)
74x2962	1	4-bit EDAC bus buffer, non- inverting, equivalent to Am2962	three- state	24	MC74F2962A (https://da tasheetspdf.com/pdf-file/ 501240/Motorola/MC74F 2961A/1)
74x2967	1	controller/driver for 16k/64k/256k dRAM		48	SN74ALS2967 (https://a rchive.org/details/bitsav ers_tidataBook_2834648 4/page/n515)
74x2968	1	controller/driver for 16k/64k/256k dRAM		48	SN74ALS2968 (https://a rchive.org/details/bitsav ers_tidataBook_2834648 4/page/n515)

74x2969	1	memory timing controller for use with EDAC			48	MC74F2969 (https://arch ive.org/details/bitsavers motoroladaSchottkyTT LData_33878952/page/n 635)
74x2970	1	memory timing controller for use without EDAC			24	MC74F2970 (https://data sheet.datasheetarchive. com/originals/distributor s/Datasheets-112/DSAP 0043139.pdf)
Part number	Units	Description	Input	Output	Pins	Datasheet
74x3004	1	selectable <u>GTL</u> voltage reference		analog	(6)	SN74GTL3004 (http://w ww.ti.com/lit/gpn/sn74gtl 3004)
74x3037	4	quad 2-input NAND gate		driver 30 Ω	16	74F3037 (https://archiv e.org/details/bitsavers_s igneticsdaManual_57966 640/page/n951)
74x3038	4	quad 2-input NAND gate		open- collector driver 30 Ω	16	74F3038 (https://archiv e.org/details/bitsavers_s igneticsdaManual_57966 640/page/n955)
74x3040	2	dual 4-input NAND gate		driver 30 Ω	16	74F3040 (https://archiv e.org/details/bitsavers_s igneticsdaManual_57966 640/page/n959)
74x3125	4	quad FET bus switch, output enable active low			(14)	SN74CBT3125 (https://a rchive.org/details/TexasI nstruments-TI-Data-CBT 5-VandCBTLV3.3-VBusS witches1998OCR/page/n 45)
74x3126	4	quad FET bus switch, output enable active high			(14)	SN74CBT3126 (https://a rchive.org/details/TexasI nstruments-TI-Data-CBT 5-VandCBTLV3.3-VBusS witches1998OCR/page/n 49)
74FCT3244	2	dual 4-bit buffer / line driver		three- state	20	IDT74FCT3244 (https://a rchive.org/details/bitsav ers_idtdataBoomanceLo gicDataBook_51362967/ page/n509)
74CBT3244, 74FST3244	2	dual 4-bit FET bus switch			20	SN74CBT3244 (https://a rchive.org/details/Texasl nstruments-TI-Data-CBT 5-VandCBTLV3.3-VBusS witches1998OCR/page/n 53) IDT74FST3244 (https://a rchive.org/details/bitsav ers_idtdataBoomanceLo gicDataBook_51362967/ page/n641)
74FCT3245	1	octal bidirectional transceiver		three- state	20	IDT74FCT3245 (https://a rchive.org/details/bitsav ers_idtdataBoomanceLo

					gicDataBook_51362967/ page/n515)
74CBT3245, 74FST3245	1	octal FET bus switch		20	SN74CBT3245A (https:// archive.org/details/Texa sInstruments-TI-Data-C BT5-VandCBTLV3.3-VB usSwitches1998OCR/pa ge/n61) IDT74FST3245 (https://a rchive.org/details/bitsav ers_idtdataBoomanceLo gicDataBook_51362967/ page/n645)
74LVX3245	1	octal bidirectional voltage- translating transceiver	three- state	(24)	74LVX3245 (https://archi ve.org/details/bitsavers_ nationaldaCROSSVOLT LowVoltageLogicSeriesD atabook_18426235/pag e/n129)
74GTLPH3245	1	32-bit LV-TTL-to-GTLP adjustable-edge-rate bus transceiver	three- state and open- collector	(114)	SN74GTLPH3245 (http s://www.mouser.com/dat asheet/2/405/sn74gtlph3 245-447892.pdf)
74x3251	1	8-line to 1-line FET multiplexer / demultiplexer		(16)	SN74CBT3251 (https://a rchive.org/details/TexasI nstruments-TI-Data-CBT 5-VandCBTLV3.3-VBusS witches1998OCR/page/n 69)
74x3253	2	dual 4-line to 1-line FET multiplexer / demultiplexer		(16)	SN74CBT3253 (https://a rchive.org/details/TexasI nstruments-TI-Data-CBT 5-VandCBTLV3.3-VBusS witches1998OCR/page/n 73)
74x3257	4	quad 2-line to 1-line FET multiplexer / demultiplexer		(16)	IDT74FST3257 (https://a rchive.org/details/bitsav ers_idtdataBoomanceLo gicDataBook_51362967/ page/n651)
74x3283	1	32-bit latchable transceiver with parity checker / generator	three- state	(120)	74ACTQ3283 (https://da tasheet.datasheetarchiv e.com/originals/distribut ors/Datasheets-22/DSA- 420818.pdf)
74x3284	1	18-bit synchronous datapath multiplexer	three- state	(100)	74ABT3284 (https://data sheet.datasheetarchive. com/originals/library/Dat asheet-019/DSA0033257 3.pdf)
74x3305	2	dual FET bus switch with extended voltage range		(8)	SN74CBT3305C (https:// www.ti.com/lit/gpn/sn74c bt3305c)
74x3306	2	dual FET bus switch		(8)	SN74CBT3306 (https://a rchive.org/details/Texasl nstruments-TI-Data-CBT 5-VandCBTLV3.3-VBusS

					witches1998OCR/page/n 85)
74x3345	1	octal FET bus switch, dual output enable		(20)	SN74CBT3345 (https://a rchive.org/details/Texasl nstruments-TI-Data-CBT 5-VandCBTLV3.3-VBusS witches1998OCR/page/n 89)
74x3374	1	8-bit metastable-resistant D- type flip-flop	three- state	20	SN74AS3374 (https://da tasheet.datasheetarchiv e.com/originals/scans/S cans-067/DSA2IH00215 569.pdf)
74x3383	1	5-bit 4-port FET bus exchange switch		24	IDT74FST3383 (https://a rchive.org/details/bitsav ers_idtdataBoomanceLo gicDataBook_51362967/ page/n655)
74x3384	2	dual 5-bit FET bus switch		24	IDT74FST3384 (https://a rchive.org/details/bitsav ers_idtdataBoomanceLo gicDataBook_51362967/ page/n509)
74x3386	1	5-bit 4-port FET bus exchange switch with extended voltage range		(24)	SN74CBT3386 (https://a rchive.org/details/Texasl nstruments-TI-Data-CBT 5-VandCBTLV3.3-VBusS witches1998OCR/page/n 113)
74x3390	1	octal 2-line to 1-line FET multiplexer / bus switch		(28)	IDT74FST3390 (https://a rchive.org/details/bitsav ers_idtdataBoomanceLo gicDataBook_51362967/ page/n665)
74x3573	1	octal transparent latch	three- state	20	IDT74FCT3573 (https://a rchive.org/details/bitsav ers_idtdataBoomanceLo gicDataBook_51362967/ page/n521)
74x3574	1	octal D-type flip flop	three- state	20	IDT74FCT3574 (https://a rchive.org/details/bitsav ers_idtdataBoomanceLo gicDataBook_51362967/ page/n527)
74x3584	2	dual 5-bit FET bus switch	25 Ω series resistor	24	QS74QST3584 (https://d atasheet.datasheetarchi ve.com/originals/distribu tors/Datasheets-111/DS AP0025436.pdf)
74x3611	1	2304-bit FIFO memory (64x36)	three- state	(120)	SN74ABT3611 (https://a rchive.org/details/bitsav ers_tidataBookeFIFOMe moriesDataBook_33517 703/page/n361)
74x3612	1	4608-bit bidirectional FIFO memory (2x64x36)	three- state	(120)	SN74ABT3612 (https://a rchive.org/details/bitsav ers_tidataBookeFIFOMe

					moriesDataBook_33517 703/page/n387)
74x3613	1	2304-bit FIFO memory (64x36)	three- state	(120)	SN74ABT3613 (https://a rchive.org/details/bitsav ers_tidataBookeFIFOMe moriesDataBook_33517 703/page/n287)
74x3614	1	4608-bit bidirectional FIFO memory (2x64x36)	three- state	(120)	SN74ABT3614 (https://a rchive.org/details/bitsav ers_tidataBookeFIFOMe moriesDataBook_33517 703/page/n319)
74x3622	1	18432-bit bidirectional FIFO memory (2x256x36)	three- state	(120)	SN74ACT3622 (https://a rchive.org/details/bitsav ers_tidataBookeFIFOMe moriesDataBook_33517 703/page/n177)
74x3631	1	18432-bit FIFO memory (512x36)	three- state	(120)	SN74ACT3631 (https://a rchive.org/details/bitsav ers_tidataBookeFIFOMe moriesDataBook_33517 703/page/n105)
74x3632	1	36864-bit bidirectional FIFO memory (2x512x36)	three- state	(120)	SN74ACT3632 (https://a rchive.org/details/bitsav ers_tidataBookeFIFOMe moriesDataBook_33517 703/page/n233)
74x3638	1	32768-bit bidirectional FIFO memory (2x512x32)	three- state	(120)	SN74ACT3638 (https://a rchive.org/details/bitsav ers_tidataBookeFIFOMe moriesDataBook_33517 703/page/n203)
74x3641	1	36864-bit FIFO memory (1024x36)	three- state	(120)	SN74ACT3641 (https://a rchive.org/details/bitsav ers_tidataBookeFIFOMe moriesDataBook_33517 703/page/n129)
74x3642	1	73728-bit bidirectional FIFO memory (2x1024x36)	three- state	(120)	SN74ACT3642 (https://a rchive.org/details/bitsav ers_tidataBookeFIFOMe moriesDataBook_33517 703/page/n259)
74x3651	1	73728-bit FIFO memory (2048x36)	three- state	(120)	SN74ACT3651 (https://a rchive.org/details/bitsav ers_tidataBookeFIFOMe moriesDataBook_33517 703/page/n153)
74x3708	1	8192-bit PROM (1024x8)	open- collector	24	SN74S3708 (https://arch ive.org/details/bitsavers _tidataBookcomputerCo mponentsDataBook_168 51665/page/n177)
74x3807	1	1-to-10 clock driver	driver	20	IDT74FCT3807 (https://a rchive.org/details/bitsav ers_idtdataBoomanceLo gicDataBook_51362967/ page/n589)

74x3827	1	10-bit buffer		three- state	24	IDT74FCT3827 (https://a rchive.org/details/bitsav ers_idtdataBoomanceLo gicDataBook_51362967/ page/n535)
74x3861	1	10-bit FET bus switch			(24)	SN74CBT3861 (https://a rchive.org/details/TexasI nstruments-TI-Data-CBT 5-VandCBTLV3.3-VBusS witches1998OCR/page/n 121)
74x3862	1	10-bit FET bus switch with dual output enable			(24)	IDT74CBTLV3862 (http s://datasheet.datasheeta rchive.com/originals/dist ributors/Datasheets-14/D SA-272858.pdf)
74x3893	1	quad <u>Futurebus</u> backplane transceiver		three- state and open- collector	(20)	MC74F3893A (https://ar chive.org/details/bitsave rs_motoroladaFASTandL STTLData_35934218/pa ge/n313)
74x3907	1	Pentium clock synthesizer		three- state	(28)	IDT74FCT3907 (https://a rchive.org/details/bitsav ers_idtdataBoomanceLo gicDataBook_51362967/ page/n629)
74x3932	1	PLL-based clock driver		three-	(48)	IDT74FCT3932 (https://a rchive.org/details/bitsav ers_idtdataBoomanceLo
				state		gicDataBook_51362967/ page/n619)
Part number	Units	Description	Input	state Output	Pins	gicDataBook_51362967/ page/n619) Datasheet
Part number 74x4002	Units	Description	Input	State Output	Pins 14	Gio_IddataDoonna rocispgicDataBook_51362967/page/n619)DatasheetCD74HC4002 (https://web.archive.org/web/20170221111335/http://www.ti.com/lit/ds/symlink/cd74hc4002.pdf)
Part number 74x4002 74x4015	Units 2 2	Description dual 4-input NOR gate dual 4-bit shift registers	Input	State Output	Pins 14 16	Gio_Iddatabolina iocisigicDataBook_51362967/page/n619)DatasheetCD74HC4002 (https://web.archive.org/web/20170221111335/http://www.ti.com/lit/ds/symlink/cd74hc4002.pdf)CD74HC4015 (https://web.archive.org/web/20170805221247/http://www.ti.com/lit/ds/symlink/cd74hc4015.pdf)
Part number 74x4002 74x4015 74x4016	Units 2 2 4	Description dual 4-input NOR gate dual 4-bit shift registers quad bilateral switch	Input	state Output analog	Pins 14 16 14	Gio_Iditata Book_51362967/gicDataBook_51362967/page/n619)DatasheetCD74HC4002 (https://web.archive.org/web/20170221111335/http://www.ti.com/lit/ds/symlink/cd74hc4002.pdf)CD74HC4015 (https://web.archive.org/web/20170805221247/http://www.ti.com/lit/ds/symlink/cd74hc4015.pdf)CD74HC4016 (https://web.archive.org/web/20170305192102/http://www.ti.com/lit/ds/symlink/cd74hc4016.pdf)
Part number 74x4002 74x4015 74x4016 74x4017	Units 2 2 4 1	Description dual 4-input NOR gate dual 4-bit shift registers quad bilateral switch 5-stage ÷10 Johnson counter	Input	state Output analog	Pins 14 16 14	Gic_JataBook_51362967/gicDataBook_51362967/page/n619)DatasheetCD74HC4002 (https://web.archive.org/web/20170221111335/http://www.ti.com/lit/ds/symlink/cd74hc4002.pdf)CD74HC4015 (https://web.archive.org/web/20170805221247/http://www.ti.com/lit/ds/symlink/cd74hc4015.pdf)CD74HC4016 (https://web.archive.org/web/20170305192102/http://www.ti.com/lit/ds/symlink/cd74hc4016.pdf)CD74HC4017 (https://web.archive.org/web/2013111151724/http://www.ti.com/lit/ds/symlink/cd74hc4017.pdf)

74x4022	1	4-stage ÷8 Johnson counter		14	SN74HC4022 (https://ar chive.org/details/bitsave rs_tidataBookogicDataB ook_23574286/page/n61 1)
74x4024	1	7-stage ripple carry binary counter		14	CD74HC4024 (https://we b.archive.org/web/20170 305193812/http://www.ti. com/lit/ds/symlink/cd74 hc4024.pdf)
74x4028	1	BCD to decimal decoder		16	TC74HC4028P (https://d atasheet.datasheetarchi ve.com/originals/scans/ Scans-067/DSA2IH0020 4191.pdf)
74x4040	1	12-stage binary ripple counter		16	SN74HC4040 (https://we b.archive.org/web/20161 104125848/http://www.ti. com/lit/ds/symlink/sn74 hc4040.pdf)
74x4046	1	phase-locked loop and voltage-controlled oscillator		16	CD74HC4046A (https://w eb.archive.org/web/2016 1130143815/http://www.t i.com/lit/ds/symlink/cd7 4hc4046a.pdf)
74x4049	6	hex inverting buffer		16	CD74HC4049 (https://we b.archive.org/web/20170 517050814/http://www.ti. com/lit/ds/symlink/cd74 hc4050.pdf)
74x4050	6	hex buffer/converter (non- inverting)		16	CD74HC4050 (https://we b.archive.org/web/20170 517050814/http://www.ti. com/lit/ds/symlink/cd74 hc4050.pdf)
74x4051	1	high-speed 8-channel analog multiplexer/demultiplexer	analog	16	CD74HC4051 (https://we b.archive.org/web/20161 213211740/http://www.ti. com/lit/ds/symlink/cd74 hc4051.pdf)
74x4052	2	dual 4-channel analog multiplexer/demultiplexers	analog	16	CD74HC4052 (https://we b.archive.org/web/20161 213211740/http://www.ti. com/lit/ds/symlink/cd74 hc4051.pdf)
74x4053	3	triple 2-channel analog multiplexer/demultiplexers	analog	16	CD74HC4053 (https://we b.archive.org/web/20161 213211740/http://www.ti. com/lit/ds/symlink/cd74 hc4051.pdf)
74x4059	1	programmable divide-by-N counter		24	CD74HC4059 (https://we b.archive.org/web/20161 104185610/http://www.ti. com/lit/ds/symlink/cd74 hc4059.pdf)
74x4060	1	14-stage binary ripple counter with oscillator		16	SN74HC4060 (https://we b.archive.org/web/20170

					306011107/http://www.ti. com/lit/ds/symlink/sn74 hc4060.pdf)
74x4061	1	14-stage asynchronous binary counter with oscillator		16	SN74HC4061 (https://ar chive.org/details/bitsave rs_tidataBookogicDataB ook_23574286/page/n44 9)
74x4066	4	quad single-pole single-throw analog switch		14	SN74HC4066 (https://we b.archive.org/web/20170 305221555/http://www.ti. com/lit/ds/symlink/sn74 hc4066.pdf)
74x4067	1	16-channel analog multiplexer/demultiplexer	ana	log 24	CD74HC4067 (https://we b.archive.org/web/20170 804052235/http://www.ti. com/lit/ds/symlink/cd74 hc4067.pdf)
74x4072	2	dual 4-input OR gate		14	TC74HC4072 (http://ww w.htmldatasheet.com/pd f/toshiba/tc74hc4072.pd f)
74x4075	3	triple 3-input OR gate		14	CD74HC4075 (http://ww w.ti.com/lit/gpn/CD74HC T4075)
74x4078	1	single 8-input OR/NOR gate		14	MM74HC4078 (https://ar chive.org/details/bitsave rs_nationaldaLogicDatab ookVolume1_95500749/ page/n701)
74x4094	1	8-bit three-state shift register/latch	threstat	ee- te 16	CD74HC4094 (https://we b.archive.org/web/20170 706105747/http://www.ti. com/lit/ds/symlink/cd74 hc4094.pdf)
74x4102	1	2-digit BCD presettable synchronous down counter		16	74HC4102 (https://datas heet.datasheetarchive.c om/originals/scans/Scan s-055/DSAIH000112054. pdf)
74x4103	1	8-bit binary presettable synchronous down counter		16	74HC4103 (https://datas heet.datasheetarchive.c om/originals/scans/Scan s-055/DSAIH000112054. pdf)
74x4245	1	8-bit 3V/5V translating transceiver	thre stat	ee- te (24)	74LVX4245 (https://archi ve.org/details/bitsavers_ nationaldaCROSSVOLT LowVoltageLogicSeriesD atabook_18426235/pag e/n135)
74x4301	1	8-bit latch, inverting	threstat	ee- te 20	MN74HC4301 (https://ar chive.org/details/bitsave rs_panasonicdicHighSpe edCMOS_23161100/pag e/n413)

74x4302	1	8-bit latch, non-inverting	three- state	20	MN74HC4302 (https://ar chive.org/details/bitsave rs_panasonicdicHighSpe edCMOS_23161100/pag e/n417)
74x4303	1	8-bit D-type flip-flop, inverting outputs	three- state	20	MN74HC4303 (https://ar chive.org/details/bitsave rs_panasonicdicHighSpe edCMOS_23161100/pag e/n421)
74x4304	1	8-bit D-type flip-flop, non- inverting outputs	three- state	20	MN74HC4304 (https://ar chive.org/details/bitsave rs_panasonicdicHighSpe edCMOS_23161100/pag e/n425)
74x4305	2	dual 4-bit buffer, inverting	three- state	20	MN74HC4305 (https://ar chive.org/details/bitsave rs_panasonicdicHighSpe edCMOS_23161100/pag e/n429)
74x4306	2	dual 4-bit buffer, non- inverting	three- state	20	MN74HC4306 (https://ar chive.org/details/bitsave rs_panasonicdicHighSpe edCMOS_23161100/pag e/n433)
74x4316	4	quad analog switch	analog	14	MM74HC4316 (https://ar chive.org/details/bitsave rs_nationaldaLogicDatab ookVolume1_95500749/ page/n703)
74x4351	1	8-channel analog multiplexer/demultiplexer with latch	analog	20	CD74HC4351 (http://ww w.ti.com/lit/gpn/cd74hc4 352)
74x4352	2	dual 4-channel analog multiplexer/demultiplexer with latch	analog	20	CD74HC4352 (http://ww w.ti.com/lit/gpn/cd74hc4 352)
74x4353	3	triple 2-channel analog multiplexer/demultiplexer with latch	analog	20	MC74HC4353 (https://ar chive.org/details/bitsave rs_motoroladaHighSpee dCMOSData_40597139/ page/n741)
74x4374	1	8-bit dual-rank synchronizer	three- state	20	SN74AS4374 (https://da tasheet.datasheetarchiv e.com/originals/scans/S cans-056/DSAIH000137 795.pdf)
74x4503	1	controller for 64k/256k/1M dynamic RAM	three- state	52	SN74ACT4503 (https://u sermanual.wiki/Docume nt/1990TICacheMemory ManagementDataBook.1 210032352.pdf)
74x4510	1	BCD decade up/down counter		16	CD74HC4510 (https://ar chive.org/details/bitsave rs_rcadataBooMOS_358 21859/page/n559)
74x4511	1	BCD to 7-segment decoder		16	CD74HC4511 (http://ww w.ti.com/lit/gpn/cd54hc4

						<u>511)</u>
74x4514	1	4-to-16 line decoder/demultiplexer, input latches			24	CD74HC4514 (http://ww w.ti.com/lit/gpn/cd54hc4 514)
74x4515	1	4-to-16 line decoder/demultiplexer with input latches; inverting			24	CD74HC4515 (http://ww w.ti.com/lit/gpn/cd54hc4 514)
74x4516	1	4-bit binary up/down counter			16	CD74HC4516 (https://ar chive.org/details/bitsave rs_rcadataBooMOS_358 21859/page/n559)
74x4518	2	dual 4-bit synchronous decade counter			16	CD74HC4518 (http://ww w.ti.com/lit/gpn/cd74hc4 520)
74x4520	2	dual 4-bit synchronous binary counter			16	CD74HC4520 (http://ww w.ti.com/lit/gpn/cd74hc4 520)
74x4538	2	dual retriggerable precision monostable multivibrator			16	CD74HC4538 (http://ww w.ti.com/lit/gpn/cd54hc4 538)
74x4543	1	BCD to 7-segment latch/decoder/driver for LCDs			16	CD74HC4543 (http://ww w.ti.com/lit/gpn/cd74hc4 543)
74x4560	1	4-bit BCD adder			16	MM74HC4560 (https://ar chive.org/details/bitsave rs_nationalda74HCDatab ook_36362852/page/n53 1)
74x4724	1	8-bit addressable latch			16	SN74HC4724 (https://ar chive.org/details/bitsave rs_tidataBookogicDataB ook_23574286/page/n45 7)
74x4764	1	programmable dRAM controller			(100)	74ABT4764 (https://data sheet.datasheetarchive. com/originals/distributor s/Datasheets-110/DSAP 0018785.pdf)
74x4799	1	Timer for NiCd and NiMH chargers	Schmitt trigger	open- collector and three- state	16	74LV4799 (https://datas heet.datasheetarchive.c om/originals/distributors/ Datasheets-25/DSA-494 778.pdf)
74x4851	1	8-channel analog multiplexer/demultiplexer		analog	16	SN74HC4851 (https://we b.archive.org/web/20160 508140402/http://www.ti. com/lit/ds/symlink/sn74 hc4851.pdf)
74x4852	2	dual 4-channel analog multiplexer/demultiplexer		analog	16	SN74HC4852 (http://ww w.ti.com/lit/gpn/sn74hc4 852)
74x5074	2	dual positive edge-triggered D-type flip-flop (metastable immune)			14	74ABT5074 (https://data sheet.datasheetarchive. com/originals/distributor

						s/Datasheets-25/DSA-49 6118.pdf)
74x5245	1	octal bidirectional transceiver	Schmitt trigger	three- state	20	DM74ALS5245 (https://a rchive.org/details/bitsav ers_nationaldaicDataboo k_22808448/page/n417)
74x5300	1	fiber optic LED driver		driver 120 mA	8	74F5300 (http://pdf.data sheetcatalog.com/datas heet/philips/N74F5300D. pdf)
74x5302	2	dual fiber optic LED / clock driver		driver 160 mA	14	74F5302 (http://www.dat asheetbank.com/datash eet-download/530792/1/ Philips/74F5302)
74x5400	1	11-bit line/memory driver, non-inverting		three- state, 25 Ω series resistor	28	SN74ABT5400 (https://a rchive.org/details/bitsav ers_tidataBookiCMOSTe chnologyDataBook_4021 7042/page/n605)
74x5401	1	11-bit line/memory driver, inverting		three- state, 25 Ω series resistor	28	SN74ABT5401 (https://a rchive.org/details/bitsav ers_tidataBookiCMOSTe chnologyDataBook_4021 7042/page/n609)
74x5402	1	12-bit line/memory driver, non-inverting		three- state, 25 Ω series resistor	28	SN74ABT5402 (https://a rchive.org/details/bitsav ers_tidataBookiCMOSTe chnologyDataBook_4021 7042/page/n613)
74x5403	1	12-bit line/memory driver, inverting		three- state, 25 Ω series resistor	28	SN74ABT5403 (https://a rchive.org/details/bitsav ers_tidataBookiCMOSTe chnologyDataBook_4021 7042/page/n617)
74x5555	1	programmable delay timer with oscillator			16	74HC5555 (https://asset s.nexperia.com/docume nts/data-sheet/74HC555 5.pdf)
74x5620	1	octal bidirectional transceiver	Schmitt trigger	three- state	20	DM74ALS5620 (https://a rchive.org/details/bitsav ers_nationaldaicDataboo k_22808448/page/n417)
Part number	Units	Description	Input	Output	Pins	Datasheet
74x6000	1	logic-to-logic optocoupler, non-inverting			6	74OL6000 (https://datas heet.datasheetarchive.c om/originals/distributors/ Datasheets-12/DSA-229 129.pdf)
74x6001	1	logic-to-logic optocoupler, inverting			6	74OL6001 (https://datas heet.datasheetarchive.c om/originals/distributors/ Datasheets-12/DSA-229 129.pdf)
74x6010	1	logic-to-logic optocoupler, non-inverting		open- collector 15 V	6	74OL6010 (https://datas heet.datasheetarchive.c om/originals/distributors/

						Datasheets-12/DSA-229 129.pdf)
74x6011	1	logic-to-logic optocoupler, inverting		open- collector 15 V	6	74OL6011 (https://datas heet.datasheetarchive.c om/originals/distributors/ Datasheets-12/DSA-229 129.pdf)
74x6300	1	programmable dynamic memory refresh timer			16	SN74ALS6300 (https://u sermanual.wiki/Docume nt/1990TICacheMemory ManagementDataBook.1 210032352.pdf)
74x6301	1	dynamic memory refresh controller, transparent and burst modes, for 16K, 64K, 256K, and 1M dRAM			52	SN74ALS6301 (https://a rchive.org/details/bitsav ers_tidataBook_2834648 4/page/n535)
74x6302	1	dynamic memory refresh controller, transparent and burst modes, for 16K, 64K, 256K, and 1M dRAM			52	SN74ALS6302 (https://a rchive.org/details/bitsav ers_tidataBook_2834648 4/page/n535)
74x6310	1	static column and page mode access detector for dRAM			20	SN74ALS6310A (https:// usermanual.wiki/Docum ent/1990TICacheMemor yManagementDataBook. 1210032352.pdf)
74x6311	1	static column and page mode access detector for dRAM			20	SN74ALS6311A (https:// usermanual.wiki/Docum ent/1990TICacheMemor yManagementDataBook. 1210032352.pdf)
74x6323	1	programmable ripple counter with oscillator		three- state	(8)	74HC6323A (https://ass ets.nexperia.com/docum ents/data-sheet/74HC_H CT6323A.pdf)
74x6364	1	64-bit flow-through error detection and correction circuit		three- state	(207)	SN74AS6364 (https://us ermanual.wiki/Documen t/1990TICacheMemoryM anagementDataBook.12 10032352.pdf)
74x6800	1	10-bit FET bus switch with precharge			24	IDT74FST6800 (https://a rchive.org/details/bitsav ers_idtdataBoomanceLo gicDataBook_51362967/ page/n671)
74x6845	1	8-bit FET bus switch with precharge and extended voltage range			(20)	SN74CBT6845C (https:// datasheet.datasheetarch ive.com/originals/distribu tors/Datasheets-36/DSA -711566.pdf)
74x7001	4	quad 2-input AND gate	Schmitt trigger		14	SN74HC7001 (http://ww w.ti.com/lit/gpn/sn74hc7 001)
74x7002	4	quad 2-input NOR gate	Schmitt trigger		14	SN74HC7002 (http://ww w.ti.com/lit/gpn/sn74hc7 002)

74x7003	4	quad 2-input NAND gate	Schmitt trigger	open- collector	14	SN74HC7003 (https://ar chive.org/details/bitsave rs_tidataBookogicDataB ook_23574286/page/n70 7)
74x7006	6	two inverters, one 3-input NAND, one 4-input NAND, one 3-input NOR, one 4-input NOR			24	SN74HC7006 (https://ar chive.org/details/bitsave rs_tidataBookSLogicDat aBook_45157566/page/n 773)
74x7007	6	hex buffer gate			14	TC74HCT7007AP (http s://www.alldatasheet.co m/datasheet-pdf/pdf/317 96/TOSHIBA/TC74HCT7 007AF.html)
74x7008	6	two inverters, three 2-input NAND, three 2-input NOR			24	SN74HC7008 (https://ar chive.org/details/bitsave rs_tidataBookSLogicDat aBook_45157566/page/n 777)
74x7014	6	hex buffer gate	Schmitt trigger		14	74HC7014 (https://asset s.nexperia.com/docume nts/data-sheet/74HC701 4.pdf)
74x7022	1	4-stage ÷8 Johnson counter with power-up clear			14	SN74HC7022 (https://ar chive.org/details/bitsave rs_tidataBookogicDataB ook_23574286/page/n61 5)
74x7030	1	576-bit FIFO memory (64x9)		three- state	28	74HC7030 (https://archiv e.org/details/highspeedc mosda00sign/page/764)
74x7032	4	quad 2-input OR gates	Schmitt trigger		14	SN74HC7032 (https://ar chive.org/details/bitsave rs_tidataBookSLogicDat aBook_45157566/page/n 787)
74x7038	1	9-bit bus transceiver with latch		three- state	24	CD74HC7038 (https://ar chive.org/details/bitsave rs_rcadataBooMOS_358 21859/page/n641)
74x7046	1	phase-locked loop with voltage-controlled oscillator and lock detector			16	CD74HC7046A (http://w ww.ti.com/lit/gpn/cd74hc 7046a)
74x7060	1	14-stage binary counter with oscillator	Schmitt trigger		20	CD74AC7060 (https://ar chive.org/details/RCA-R CAAdvancedCMOSLogi cICs1987OCR/page/n29 1)
74x7074	6	two inverters, one 2-input NAND, one 2-input NOR, two D-type flip-flops			24	SN74HC7074 (https://ar chive.org/details/bitsave rs_tidataBookSLogicDat aBook_45157566/page/n 791)
74x7075	6	two inverters, two 2-input NAND, two D-type flip-flops			24	SN74HC7075 (https://ar chive.org/details/bitsave rs_tidataBookSLogicDat

						aBook_45157566/page/n 797)
74x7076	6	two inverters, two 2-input NOR, two D-type flip-flops			24	SN74HC7076 (https://ar chive.org/details/bitsave rs_tidataBookSLogicDat aBook_45157566/page/n 803)
74x7080	1	16-bit parity generator / checker			20	74HCT7080 (https://data sheet.datasheetarchive. com/originals/distributor s/Datasheets-25/DSA-49 1964.pdf)
74x7132	4	quad adjustable comparator with output latches	Schmitt trigger	three- state	14	74HCT7132 (https://data sheet.datasheetarchive. com/originals/distributor s/Datasheets-30/DSA-59 6949.pdf)
74x7200	1	2304-bit FIFO memory (256x9)			28	SN74ACT7200L (https:// archive.org/details/bitsa vers_tidataBookeFIFOM emoriesDataBook_3351 7703/page/n695)
74x7201	1	4608-bit FIFO memory (512x9)			28	SN74ACT7201LA (http s://archive.org/details/bit savers_tidataBookeFIF OMemoriesDataBook_3 3517703/page/n695)
74x7202	1	9216-bit FIFO memory (1024x9)			28	SN74ACT7202LA (http s://archive.org/details/bit savers_tidataBookeFIF OMemoriesDataBook_3 3517703/page/n695)
74x7203	1	18432-bit FIFO memory (2048x9)			28	SN74ACT7203L (https:// archive.org/details/bitsa vers_tidataBookeFIFOM emoriesDataBook_3351 7703/page/n715)
74ACT7204	1	36864-bit FIFO memory (4096x9)			28	SN74ACT7204L (https:// archive.org/details/bitsa vers_tidataBookeFIFOM emoriesDataBook_3351 7703/page/n715)
74HCU7204	2	dual unbuffered inverters			(8)	SN74HCU7204 (http://w ww.ti.com/lit/gpn/sn74hc u7204)
74x7205	1	73728-bit FIFO memory (8192x9)			28	SN74ACT7205L (https:// datasheet.datasheetarch ive.com/originals/distribu tors/Datasheets-36/DSA -705735.pdf)
74x7206	1	147456-bit FIFO memory (16384x9)			28	SN74ACT7206L (https:// datasheet.datasheetarch ive.com/originals/distribu tors/Datasheets-36/DSA -705735.pdf)
74x7240	1	octal bus buffer, inverting	Schmitt trigger	three- state	20	TC74HC7240AP (http://p df.datasheet.live/datash

						eets-1/toshiba/TC74HC7 241AP.pdf)
74x7241	1	octal bus buffer, non- inverting	Schmitt trigger	three- state	20	TC74HC7241AP (http://p df.datasheet.live/datash eets-1/toshiba/TC74HC7 241AP.pdf)
74x7244	1	octal bus buffer, non- inverting	Schmitt trigger	three- state	20	TC74HC7244AP (http://p df.datasheet.live/datash eets-1/toshiba/TC74HC7 241AP.pdf)
74x7245	1	octal bus transceiver, non- inverting	Schmitt trigger	three- state	20	M74HC7245 (https://pdf 1.alldatasheet.com/data sheet-pdf/view/23130/ST MICROELECTRONICS/ M74HC7645.html)
74x7266	4	quad 2-input XNOR gate			14	SN74HC7266 (https://ar chive.org/details/bitsave rs_tidataBookogicDataB ook_23574286/page/n46
74x7273	8	octal positive edge-triggered D-type flip-flop with reset		open- collector	20	74HCT7273 (https://data sheet.datasheetarchive. com/originals/distributor s/Datasheets-25/DSA-49 6043.pdf)
74x7292	1	programmable divider/timer			16	TC74HC7292AP (https:// pdf1.alldatasheet.com/d atasheet-pdf/view/3177 1/TOSHIBA/TC74HC729 2AP.html)
74x7294	1	programmable divider/timer			16	M74HC7294 (https://pdf 1.alldatasheet.com/data sheet-pdf/view/23075/ST MICROELECTRONICS/ M74HC7294.html)
74x7340	1	8-bit bus driver with bidirectional registers		three- state	24	SN74HC7340 (https://ar chive.org/details/bitsave rs_tidataBookogicDataB ook_23574286/page/n62 5)
74x7403	1	256-bit FIFO memory (64x4)		three- state	16	74HC7403 (http://pdf.dat asheetcatalog.com/data sheet/philips/74HC7403. pdf)
74x7404	1	320-bit FIFO memory (64x5)		three- state	18	74HC7404 (https://pdf1. alldatasheet.com/datash eet-pdf/view/15661/PHIL IPS/74HC7404.html)
74x7540	8	octal buffer/line driver, inverting	Schmitt trigger	three- state	20	74HC7540 (https://asset s.nexperia.com/docume nts/data-sheet/74HC_HC T7540.pdf)
74x7541	8	octal buffer/line driver, non- inverting	Schmitt trigger	three- state	20	74HC7541 (https://asset s.nexperia.com/docume nts/data-sheet/74HC_HC T7541.pdf)

74x7597	1	8-bit shift register with input latches			16	74HC7597 (http://pdf.dat asheetcatalog.com/data sheet/philips/74HC7597. pdf)
74x7623	1	octal bus transceiver, non- inverting		three- state and open- drain	20	CD74AC7623 (https://ar chive.org/details/RCA-R CAAdvancedCMOSLogi clCs1987OCR/page/n29 3)
74x7640	1	octal bus transceiver, inverting	Schmitt trigger	three- state	20	M74HC7640 (https://pdf 1.alldatasheet.com/data sheet-pdf/view/23130/ST MICROELECTRONICS/ M74HC7645.html)
74x7643	1	octal bus transceiver, non- inverting/inverting	Schmitt trigger	three- state	20	M74HC7643 (https://pdf 1.alldatasheet.com/data sheet-pdf/view/23130/ST MICROELECTRONICS/ M74HC7645.html)
74x7645	1	octal bus transceiver, non- inverting	Schmitt trigger	three- state	20	M74HC7645 (https://pdf 1.alldatasheet.com/data sheet-pdf/view/23130/ST MICROELECTRONICS/ M74HC7645.html)
74x7731	4	quad 64-bit static shift register			16	74HC7731 (http://pdf.dat asheetcatalog.com/data sheet/philips/74HCT773 1.pdf)
74x7793	1	8-bit noninverting transparent latch with readback		three- state	20	MC74HC7793 (https://da tasheet.datasheetarchiv e.com/originals/distribut ors/Datasheets-112/DSA P0048904.pdf)
74x7801	1	18432-bit FIFO memory (1024x18), clocked		three- state	(68)	SN74ACT7801 (https://a rchive.org/details/bitsav ers_tidataBookeFIFOMe moriesDataBook400_13 134187/page/n21)
74x7802	1	18432-bit FIFO memory (1024x18)		three- state	(68)	SN74ACT7802 (https://a rchive.org/details/bitsav ers_tidataBookeFIFOMe moriesDataBook400_13 134187/page/n115)
74x7803	1	9216-bit FIFO memory (512x18), clocked		three- state	(56)	SN74ACT7803 (https://a rchive.org/details/bitsav ers_tidataBookeFIFOMe moriesDataBook400_13 134187/page/n37)
74x7804	1	9216-bit FIFO memory (512x18)		three- state	(56)	SN74ACT7804 (https://a rchive.org/details/bitsav ers_tidataBookeFIFOMe moriesDataBook400_13 134187/page/n127)
74x7805	1	4608-bit FIFO memory (256x18), clocked		three- state	(56)	SN74ACT7805 (https://a rchive.org/details/bitsav ers_tidataBookeFIFOMe

						moriesDataBook400_13 134187/page/n51)
74x7806	1	4608-bit FIFO memory (256x18)	tis	three- state	(56)	SN74ACT7806 (https://a rchive.org/details/bitsav ers_tidataBookeFIFOMe moriesDataBook400_13 134187/page/n139)
74x7807	1	18432-bit FIFO memory (2048x9), clocked	tis	three- state	(44)	SN74ACT7807 (https://a rchive.org/details/bitsav ers_tidataBookeFIFOMe moriesDataBook400_13 134187/page/n65)
74x7808	1	18432-bit FIFO memory (2048x9)	ti s	three- state	(44)	SN74ACT7808 (https://a rchive.org/details/bitsav ers_tidataBookeFIFOMe moriesDataBook400_13 134187/page/n151)
74x7811	1	18432-bit FIFO memory (1024x18), clocked	ti s	three- state	(68)	SN74ACT7811 (https://a rchive.org/details/bitsav ers_tidataBookeFIFOMe moriesDataBook400_13 134187/page/n81)
74x7813	1	1152-bit FIFO memory (64x18), clocked	ti s	three- state	(56)	SN74ACT7813 (https://a rchive.org/details/bitsav ers_tidataBookeFIFOMe moriesDataBook400_13 134187/page/n99)
74x7814	1	1152-bit FIFO memory (64x18)	tis	three- state	(56)	SN74ACT7814 (https://a rchive.org/details/bitsav ers_tidataBookeFIFOMe moriesDataBook400_13 134187/page/n165)
74x7815	1	4608-bit bidirectional FIFO memory(2x64x36)	tis	three- state	(120)	SN74ABT7815 (https://a rchive.org/details/bitsav ers_tidataBookeFIFOMe moriesDataBook400_13 134187/page/n279)
74x7816	1	4608-bit bidirectional FIFO memory(2x64x36)	tis	three- state	(120)	SN74ABT7816 (https://a rchive.org/details/bitsav ers_tidataBookeFIFOMe moriesDataBook400_13 134187/page/n291)
74x7817	1	2304-bit FIFO memory(64x36)	ti s	three- state	(120)	SN74ABT7817 (https://a rchive.org/details/bitsav ers_tidataBookeFIFOMe moriesDataBook400_13 134187/page/n293)
74x7818	1	2304-bit FIFO memory(64x36)	ti s	three- state	(120)	SN74ABT7818 (https://a rchive.org/details/bitsav ers_tidataBookeFIFOMe moriesDataBook400_13 134187/page/n295)
74x7819	1	18432-bit bidirectional FIFO memory (2x512x18), clocked	ti	three- state	(80)	SN74ABT7819 (https://a rchive.org/details/bitsav ers_tidataBookeFIFOMe moriesDataBook400_13 134187/page/n207)

74x7	820	1	18432-bit bidirectional FIFO t memory (2x512x18) s		three- state	(80)	SN74ABT7820 (https://a rchive.org/details/bitsav ers_tidataBookeFIFOMe moriesDataBook400_13 134187/page/n229)
74x7	821	1	32768-bit bidirectional FIFO th memory (2x512x32) si		three- state	(120)	SN74ACT7821 (https://a rchive.org/details/bitsav ers_tidataBookeFIFOMe moriesDataBook400_13 134187/page/n317)
74x7	822	1	32768-bit bidirectional FIFO t memory (2x512x32), clocked s		three- state	(120)	SN74ACT7822 (https://a rchive.org/details/bitsav ers_tidataBookeFIFOMe moriesDataBook400_13 134187/page/n325)
74x7	823	1	36864-bit FIFO memory (1024x36), clocked	6864-bit FIFO memory thre 1024x36), clocked stat		(120)	SN74ACT7823 (https://a rchive.org/details/bitsav ers_tidataBookeFIFOMe moriesDataBook400_13 134187/page/n333)
74x7	881	1	18432-bit FIFO memory (1024x18), clocked		three- state	(68)	SN74ACT7881 (https://a rchive.org/details/bitsav ers_tidataBookeFIFOMe moriesDataBook_33517 703/page/n479)
74x7	882	1	36864-bit FIFO memory (2048x18), clocked		three- state	(68)	SN74ACT7882 (https://a rchive.org/details/bitsav ers_tidataBookeFIFOMe moriesDataBook_33517 703/page/n495)
74x7	884	1	73728-bit FIFO memory (4096x18), clocked		three- state	(68)	SN74ACT7884 (https://a rchive.org/details/bitsav ers_tidataBookeFIFOMe moriesDataBook_33517 703/page/n511)
74x8	003	2	dual 2-input NAND gate			8	SN74ALS8003 (https://a rchive.org/details/bitsav ers_tidataBookVol3_258 40031/page/n771)
74x8	151	1	10-bit inverting/non-inverting buffer	Schmitt trigger	three- state	24	SN74LV8151 (http://ww w.ti.com/lit/gpn/sn74lv81 51)
74x8	153	1	8-bit serial-to-parallel interface		three- state or open- collector	20	SN74LV8153 (http://ww w.ti.com/lit/gpn/sn74lv81 53)
74x8	154	2	dual 16-bit counters with output registers		three- state	20	SN74LV8154 (http://ww w.ti.com/lit/gpn/sn74lv81 54)
74x8	161	1	8-bit synchronous binary counter			24	SN74ALS8161 (https://d atasheet.datasheetarchi ve.com/originals/scans/ Scans-067/DSA2IH0021 5541.pdf)
74x8	240	1	octal inverting buffer with JTAG port		three- state	24	SN74BCT8240A (https:// archive.org/details/bitsa vers_tidataBookLogicDa

						taBook_44713328/page/ n23)
74x8244	1	octal non-inverting buffer with <u>JTAG</u> port		three- state	24	SN74BCT8244A (https:// archive.org/details/bitsa vers_tidataBookLogicDa taBook_44713328/page/ n43)
74x8245	1	octal bus transceiver with JTAG port	octal bus transceiver with JTAG port		24	SN74ABT8245 (https://a rchive.org/details/bitsav ers_tidataBookiCMOSTe chnologyDataBook_4021 7042/page/n735)
74x8373	1	octal D-type latch with <u>JTAG</u> port		three- state	24	SN74BCT8373A (https:// archive.org/details/bitsa vers_tidataBookLogicDa taBook_44713328/page/ n85)
74x8374	1	octal D-type edge-triggered flip-flop with <u>JTAG</u> port		three- state	24	SN74BCT8374A (https:// archive.org/details/bitsa vers_tidataBookLogicDa taBook_44713328/page/ n105)
74x8400	1	expandable error checker / corrector		three- state	48	SN74ALS8400 (https://a rchive.org/details/bitsav ers_tidataBook_2834648 4/page/n541)
74x8541	1	8-bit buffer, selectable inverting/non-inverting	Schmitt trigger	three- state	20	SN74AHC8541 (https://d atasheet.datasheetarchi ve.com/originals/distribu tors/DKDS41/DSANUW W0029467.pdf)
74x8543	1	octal registered bus transceiver with JTAG port		three- state	28	SN74ABT8543 (https://a rchive.org/details/bitsav ers_tidataBookiCMOSTe chnologyDataBook_4021 7042/page/n757)
74x8646	1	octal bus transceiver and register with JTAG port		three- state	28	SN74ABT8646 (https://a rchive.org/details/bitsav ers_tidataBookiCMOSTe chnologyDataBook_4021 7042/page/n765)
74x8652	1	octal bus transceiver and register with JTAG port		three- state	28	SN74ABT8652 (https://a rchive.org/details/bitsav ers_tidataBookiCMOSTe chnologyDataBook_4021 7042/page/n775)
74x8818	1	16-bit microprogram sequencer, cascadable		three- state	(84)	SN74ACT8818 (https://a rchive.org/details/bitsav ers_tidataBookamily32Bi tCMOSProcessorBuildin gBlocksDat_39357329/p age/n19)
74x8832	1	32-bit registered ALU		three- state	(208)	SN74ACT8832 (https://a rchive.org/details/bitsav ers_tidataBookamily32Bi tCMOSProcessorBuildin

					gBlocksDat_39357329/p age/n79)
74x8834	1	40-bit register file	three- state	(156)	SN74AS8834 (https://ar chive.org/details/bitsave rs_tidataBook_2834648 4/page/n545)
74x8835	1	16-bit microprogram sequencer, cascadable	three- state	(156)	SN74AS8835 (https://da tasheet.datasheetarchiv e.com/originals/distribut ors/Datasheets-112/DSA P0053260.pdf)
74x8836	1	32x32-bit multiplier/accumulator	three- state	(156)	SN74ACT8836 (https://a rchive.org/details/bitsav ers_tidataBookamily32Bi tCMOSProcessorBuildin gBlocksDat_39357329/p age/n273)
74x8837	1	64-bit floating point unit	three- state	(208)	SN74ACT8837 (https://a rchive.org/details/bitsav ers_tidataBookamily32Bi tCMOSProcessorBuildin gBlocksDat_39357329/p age/n307)
74x8838	1	64-bit barrel shifter	three- state	(84)	SN74AS8838 (https://ar chive.org/details/bitsave rs_tidataBook_2834648 4/page/n555)
74x8839	1	32-bit shuffle/exchange network	three- state	(85)	SN74AS8839 (https://da tasheet.datasheetarchiv e.com/originals/distribut ors/Datasheets-112/DSA P0053259.pdf)
74x8840	1	digital crossbar switch	three- state	(156)	SN74AS8840 (https://da tasheet.datasheetarchiv e.com/originals/distribut ors/Datasheets-110/DSA P0010220.pdf)
74x8841	1	digital crossbar switch	three- state	(156)	SN74ACT8841 (https://a rchive.org/details/bitsav ers_tidataBookamily32Bi tCMOSProcessorBuildin gBlocksDat_39357329/p age/n435)
74x8847	1	64-bit floating point and integer unit	three- state	(208)	SN74ACT8847 (https://a rchive.org/details/bitsav ers_tidataBookamily32Bi tCMOSProcessorBuildin gBlocksDat_39357329/p age/n461)
74x8867	1	32-bit vector processor unit	three- state	(208)	SN74ACT8867 (https://a rchive.org/details/TexasI nstruments-TI-Data-SN7 4ACT8800Family32-BitC MOSProcessorBuildingB locks19900CR/page/n49 5)

74x8952	1	octal registered bus transceiver with <u>JTAG</u> port s		three- state	28	SN74ABT8952 (https://a rchive.org/details/bitsav ers_tidataBookiCMOSTe chnologyDataBook_4021 7042/page/n785)
74x8960	1	8-bit bidirectional latched FutureBus transceiver, inverting	B-bit bidirectional latched st FutureBus transceiver, au nverting op		28	74F8960 (https://cdn.dat asheetspdf.com/pdf-dow n/7/4/F/74F8960_Philips Semiconductors.pdf)
74x8961	1	8-bit bidirectional latched FutureBus transceiver, non- inverting	8-bit bidirectional latched FutureBus transceiver, non- inverting		28	74F8961 (https://cdn.dat asheetspdf.com/pdf-dow n/7/4/F/74F8960_Philips Semiconductors.pdf)
74x8962	1 9-bit bidirectional latched state 1 FutureBus transceiver, inverting operation		three- state and open- collector	(44)	74F8962 (https://cdn.dat asheetspdf.com/pdf-dow n/7/4/F/74F8962_Philips Semiconductors.pdf)	
74x8963	1	9-bit bidirectional latched thr 1 FutureBus transceiver, non-inverting an op co		three- state and open- collector	(44)	74F8963 (https://cdn.dat asheetspdf.com/pdf-dow n/7/4/F/74F8962_Philips Semiconductors.pdf)
74x8965	9-bit bidirectional latched 1 <u>FutureBus</u> transceiver, latch select		three- state and open- collector	(44)	74F8965 (https://cdn.dat asheetspdf.com/pdf-dow n/7/4/F/74F8965_Philips Semiconductors.pdf)	
74x8966	1	9-bit bidirectional latched FutureBus transceiver, idle arbitration request / output		three- state and open- collector	(44)	74F8966 (https://cdn.dat asheetspdf.com/pdf-dow n/7/4/F/74F8965_Philips Semiconductors.pdf)
74x8980	1	JTAG test access port master with 8-bit host interface		three- state	24	SN74LVT8980 (https://ar chive.org/details/bitsave rs_tidataBookLogicData Book_44713328/page/n7 95)
74x8986	1	linkable, multidrop- addressable JTAG transceiver		three- state	(64)	SN74LVT8986 (http://ww w.ti.com/lit/gpn/sn74lvt8 986)
74x8990	1	JTAG test access port master with 16-bit host interface		three- state	(44)	SN74ACT8990 (https://a rchive.org/details/bitsav ers_tidataBookLogicDat aBook_44713328/page/n 825)
74x8994	1	JTAG scan-controlled logic/signature analyzer			(28)	SN74ACT8994 (https://a rchive.org/details/bitsav ers_tidataBookLogicDat aBook_44713328/page/n 837)
74x8996	1	multidrop-addressable JTAG transceiver			24	SN74ABT8996 (https://a rchive.org/details/bitsav ers_tidataBookLogicDat
					1	

						aBook_44713328/page/n 847)
74x8997	1	scan-controlled JTAG concatenator		three- state	28	SN74ACT8997 (https://a rchive.org/details/bitsav ers_tidataBookLogicDat aBook_44713328/page/n 887)
74x8999	1	scan-controlled JTAG multiplexer		three- state	28	SN74ACT8999 (https://a rchive.org/details/bitsav ers_tidataBookLogicDat aBook_44713328/page/n 911)
74x9000	1	programmable timer with oscillator			20	MC74HC9000 (https://da tasheet.datasheetarchiv e.com/originals/distribut ors/Datasheets-112/DSA P0048905.pdf)
74x9014	9	nine-wide buffer/line driver, inverting	Schmitt trigger		20	74HC9014 (http://pdf.dat asheetcatalog.com/data sheet/philips/74HCT901 4.pdf)
74x9015	9	nine-wide buffer/line driver, non-inverting	Schmitt trigger		20	74HC9015 (http://pdf.dat asheetcatalog.com/data sheet/philips/74HC9015. pdf)
74x9034	9	nine-wide buffer, inverting			20	MC74HC9034 (https://da tasheet.datasheetarchiv e.com/originals/distribut ors/Datasheets-112/DSA P0048907.pdf)
74x9035	9	nine-wide buffer, noninverting			20	MC74HC9035 (https://da tasheet.datasheetarchiv e.com/originals/distribut ors/Datasheets-112/DSA P0048907.pdf)
74x9046	1	PLL with band gap controlled VCO			16	74HCT9046 (https://ass ets.nexperia.com/docum ents/data-sheet/74HCT9 046A.pdf)
74x9114	9	nine-wide inverter	Schmitt trigger	open- collector	20	74HC9114 (https://asset s.nexperia.com/docume nts/data-sheet/74HC_HC T9114.pdf)
74x9115	9	nine-wide buffer	Schmitt trigger	open- collector	20	74HC9115 (https://asset s.nexperia.com/docume nts/data-sheet/74HC911 5.pdf)
74x9134	9	nine-wide buffer, inverting		open- collector	20	MC74HC9134 (https://da tasheet.datasheetarchiv e.com/originals/distribut ors/Datasheets-112/DSA P0048910.pdf)
74x9135	9	nine-wide buffer, noninverting		open- collector	20	MC74HC9135 (https://da tasheet.datasheetarchiv e.com/originals/distribut ors/Datasheets-112/DSA P0048910.pdf)

Part number	Units	Description	Input	Output	Pins	Datasheet
74x40105	1	64-bit FIFO memory (16x4)		three- state	16	CD74HC40105 (http://w ww.ti.com/lit/gpn/cd74hc 40105)
74x40104	4	4-bit bidirectional universal shift register		three- state	16	CD74HC40104 (https://a rchive.org/details/bitsav ers_rcadataBooMOS_35 821859/page/n613)
74x40103	1	presettable 8-bit synchronous down counter			16	CD74HC40103 (https://w eb.archive.org/web/2016 1104125904/http://www.t i.com/lit/ds/symlink/cd7 4hc40103.pdf)
74x40102	1	presettable synchronous 2- decade BCD down counter			16	CD74HC40102 (https://a rchive.org/details/bitsav ers_rcadataBooMOS_35 821859/page/n603)
74x9595	1	8-bit shift register with latch (serial in, parallel out)	Schmitt trigger		(16)	TC74VHC9595 (https://d atasheet.datasheetarchi ve.com/originals/distribu tors/Datasheets-SFU3/D SASFU100040801.pdf)
74x9541	1	8-bit buffer / line driver, inverting / non-inverting	Schmitt trigger	three- state	(20)	74AHC9541A (https://as sets.nexperia.com/docu ments/data-sheet/74AH C9541A.pdf)
74x9510	1	16×16-bit multiplier/accumulator (compatible to <u>Am29510</u> and TDC1010)		three- state	(68)	74HC9510 ^{[9]:534}
74x9323	1	programmable ripple counter with oscillator	programmable ripple counter three- with oscillator state		(8)	74HC9323A (http://pdf.d atasheetcatalog.com/dat asheet/philips/74HCT77 31.pdf)
74x9245	1	9-bit bidirectional transceiver, non-inverting	9-bit bidirectional transceiver, three- non-inverting state		24	74FR9245 (https://datas heet.datasheetarchive.c om/originals/distributors/ Datasheets-11/DSA-203 499.pdf)
74x9244	1	9-bit buffer / line driver, non- inverting		three- state	24	74FR9244 (https://datas heet.datasheetarchive.c om/originals/distributors/ Datasheets-11/DSA-212 907.pdf)
74x9240	1	9-bit buffer / line driver, inverting		three- state	24	74FR9240 (https://datas heet.datasheetarchive.c om/originals/distributors/ Datasheets-11/DSA-211 521.pdf)
74x9164	1	8-bit shift register (serial in/out, parallel in/out)	8-bit shift register (serial in/out, parallel in/out) Schmitt three-state		(16)	TC74VHC9164 (https://d atasheet.datasheetarchi ve.com/originals/distribu tors/Datasheets-SFU3/D SASFU100040800.pdf)

Smaller footprints

As board designs have migrated away from large amounts of logic chips, so has the need for many of the same gate in one package. Since about 1996, ^[12] there has been an ongoing trend towards one / two / three logic gates per chip. Now logic can be placed where it is physically needed on a board, instead of running long signal traces to a full-size logic chip that has many of the same gate. ^[13]

All chips in the following sections are available 5- to 10-pin <u>surface-mount packages</u>. The right digits, after the 1G/2G/3G, typically has the same functional features as older legacy chips, except for the multifunctional chips and 4-digit chip numbers, which are unique to these newer families. The "x" in the part number is a place holder for the logic family name. For example, 74x1G14 in "LVC" logic family would be "74LVC1G14". The previously stated prefixes of "SN-" and "MC-" are used to denote manufacturers, Texas Instruments and ON Semiconductor respectively.^{[14][15][16]}

Some of the manufacturers that make these smaller IC chips are: <u>Diodes Incorporated</u>, <u>Nexperia</u> (<u>NXP</u> <u>Semiconductors</u>), <u>ON Semiconductor</u> (Fairchild Semiconductor), <u>Texas Instruments</u> (<u>National</u> <u>Semiconductor</u>), <u>Toshiba</u>.

The <u>logic families</u> available in small footprints are: AHC, AHCT, AUC, AUP, AXP, HC, HCT, LVC, VHC, NC7S, NC7ST, NC7SU, NC7SV. The LVC family is very popular in small footprints because it supports the most common logic voltages of 1.8 V, 3.3 V, 5 V, its inputs are 5 V tolerant when the device is powered at a lower voltage, and an output drive of 24 mA. Gates that are commonly available across most small footprint families are 00, 02, 04, 08, 14, 32, 86, 125, 126.

One-gate chips

All chips in this section have one gate, noted by the "1G" in the part numbers.

Part number	Description	Input	Output	Pins	Datasheet
74x1G00	single 2-input NAND gate			5	LVC (https://assets.nexperi a.com/documents/data-shee t/74LVC1G00.pdf)
74x1G02	single 2-input NOR gate			5	LVC (https://assets.nexperi a.com/documents/data-shee t/74LVC1G02.pdf)
74x1G04	single inverter gate			5	LVC (https://assets.nexperi a.com/documents/data-shee t/74LVC1G04.pdf)
74x1G06	single inverter gate		open- drain	5	LVC (https://assets.nexperi a.com/documents/data-shee t/74LVC1G06.pdf)
74x1G07	single <u>buffer gate</u>		open- drain	5	LVC (https://assets.nexperi a.com/documents/data-shee t/74LVC1G07.pdf)
74x1G08	single 2-input AND gate			5	LVC (https://assets.nexperi a.com/documents/data-shee t/74LVC1G08.pdf)
74x1G09	single 2-input AND gate		open- drain	5	AUP (https://assets.nexperi a.com/documents/data-shee t/74AUP1G09.pdf)
74x1G10	single 3-input NAND gate			6	LVC (https://assets.nexperi a.com/documents/data-shee t/74LVC1G10.pdf)
74x1G11	single 3-input AND gate			6	LVC (https://assets.nexperi a.com/documents/data-shee t/74LVC1G11.pdf)
74x1G14	single inverter gate	schmitt trigger		5	LVC (https://assets.nexperi a.com/documents/data-shee t/74LVC1G14.pdf)
74x1G17	single buffer gate	schmitt trigger		5	LVC (https://assets.nexperi a.com/documents/data-shee t/74LVC1G17.pdf)
74x1G18	single 1-of-2 non-inverting demultiplexer, deselected output is 3-state		three- state	6	LVC (https://assets.nexperi a.com/documents/data-shee t/74LVC1G18.pdf)
74x1G19	single 1-to-2 <u>line decoder</u> , active low outputs			6	LVC (https://assets.nexperi a.com/documents/data-shee t/74LVC1G19.pdf)
74x1G27	single 3-input NOR gate			6	LVC (https://assets.nexperi a.com/documents/data-shee t/74LVC1G27.pdf)
74x1G29	single 2-to-3 line decoder, active low outputs			8	LVC (http://www.ti.com/lit/gp n/sn74lvc1g29)
74x1G32	single 2-input OR gate			5	LVC (https://assets.nexperi a.com/documents/data-shee t/74LVC1G32.pdf)
74x1G34	single buffer gate			5	LVC (https://assets.nexperi a.com/documents/data-shee t/74LVC1G34.pdf)

74x1G38	single 2-input NAND gate		open- drain	5	LVC (https://assets.nexperi a.com/documents/data-shee t/74AUP1G38.pdf)
74x1G57	single configurable 7-function gate	schmitt trigger		6	LVC (https://assets.nexperi a.com/documents/data-shee t/74LVC1G57.pdf)
74x1G58	single configurable 7-function gate	schmitt trigger		6	LVC (https://assets.nexperi a.com/documents/data-shee t/74LVC1G58.pdf)
74x1G66	single SPST analog switch	analog	analog	5	LVC (https://assets.nexperi a.com/documents/data-shee t/74LVC1G66.pdf)
74x1G74	single D-typ <u>e</u> flip-flop, positive-edge trigger, Q & Q outputs, asynchronous preset and clear			8	LVC (https://assets.nexperi a.com/documents/data-shee t/74LVC1G74.pdf)
74x1G79	single D-type flip-flop, positive-edge trigger, Q output			5	LVC (https://assets.nexperi a.com/documents/data-shee t/74LVC1G79.pdf)
74x1G80	single <u>D-type</u> flip-flop, positive-edge trigger, \overline{Q} output			5	LVC (https://assets.nexperi a.com/documents/data-shee t/74LVC1G80.pdf)
74x1G86	single 2-input <u>XOR gate</u> (a.k.a. 2-bit even-parity generator)			5	LVC (https://assets.nexperi a.com/documents/data-shee t/74LVC1G86.pdf)
74x1G97	single configurable 7-function gate	schmitt trigger		6	LVC (https://assets.nexperi a.com/documents/data-shee t/74LVC1G97.pdf)
74x1G98	single configurable 7-function gate	schmitt trigger		6	LVC (https://assets.nexperi a.com/documents/data-shee t/74LVC1G98.pdf)
74x1G99	single configurable 15-function gate, active-low enable	schmitt trigger	three- state	8	LVC (https://assets.nexperi a.com/documents/data-shee t/74LVC1G99.pdf)
74x1G123	single retriggerable monostable multivibrator, active-low clear			8	LVC (https://assets.nexperi a.com/documents/data-shee t/74LVC1G123.pdf)
74x1G125	single buffer gate, active-low enable		three- state	5	LVC (https://assets.nexperi a.com/documents/data-shee t/74LVC1G125.pdf)
74x1G126	single buffer gate, active-high enable		three- state	5	LVC (https://assets.nexperi a.com/documents/data-shee t/74LVC1G126.pdf)
74x1G132	single 2-input NAND gate	schmitt trigger		5	LVC (http://www.ti.com/lit/gp n/sn74lvc1g132)
74x1G139	single 2-to-4 line decoder, active low outputs			8	LVC (http://www.ti.com/lit/gp n/sn74lvc1g139)
74x1G157	single 2-input multiplexer	schmitt trigger		6	LVC (https://assets.nexperi a.com/documents/data-shee t/74LVC1G157.pdf)
74x1G158	single 2-input multiplexer, inverted output	schmitt trigger		6	AUP (https://assets.nexperi a.com/documents/data-shee t/74AUP1G158.pdf)

74x1G175	single D-type flip-flop, positive-edge trigger, Q output, asynchronous clear			6	LVC (http://www.ti.com/lit/ds/ symlink/sn74lvc1g175.pdf)
74x1G240	single inverter gate, active-low enable		three- state	5	LVC (https://assets.nexperi a.com/documents/data-shee t/74LVC1G240.pdf)
74x1G332	single 3-input OR gate			6	LVC (https://assets.nexperi a.com/documents/data-shee t/74LVC1G332.pdf)
74x1G373	single D-type transparent latch, negative-edge latching, Q output, active-low enable		three- state	6	LVC (http://www.ti.com/lit/gp n/sn74lvc1g373)
74x1G374	single D-type flip-flop, positive-edge trigger, Q output, active-low enable		three- state	6	LVC (http://www.ti.com/lit/gp n/sn74lvc1g374)
74x1G386	single 3-input XOR Gate (a.k.a. 3- bit even-parity generator)			6	LVC (https://assets.nexperi a.com/documents/data-shee t/74LVC1G386.pdf)
74x1G0832	single 3-input AND-OR combo gate (2-input AND into 2-input OR)	schmitt trigger		6	LVC (http://www.ti.com/lit/gp n/sn74lvc1g0832,)
74x1G3157	single SPDT analog switch	analog	analog	6	LVC (http://www.ti.com/lit/gp n/sn74lvc1g3157)
74x1G3208	single 3-input OR-AND combo gate (2-input OR into 2-input AND)	schmitt trigger		6	LVC (http://www.ti.com/lit/gp n/sn74lvc1g3208)

Two-gate chips

All chips in this section have two gates, noted by the "2G" in the part numbers.

Part number	Description	Input	Output	Pins	Datasheet
74x2G00	dual 2-input NAND gate			8	LVC (https://assets.nexperia.com/ documents/data-sheet/74LVC2G0 0.pdf)
74x2G02	dual 2-input NOR gate			8	LVC (https://assets.nexperia.com/ documents/data-sheet/74LVC2G0 2.pdf)
74x2G04	dual inverter gate			6	LVC (https://assets.nexperia.com/ documents/data-sheet/74LVC2G0 4.pdf)
74x2G06	dual inverter gate		open- drain	6	LVC (https://assets.nexperia.com/ documents/data-sheet/74LVC2G0 6.pdf)
74x2G07	dual buffer gate		open- drain	6	LVC (https://assets.nexperia.com/ documents/data-sheet/74LVC2G0 7.pdf)
74x2G08	dual 2-input AND gate			8	LVC (https://assets.nexperia.com/ documents/data-sheet/74LVC2G0 8.pdf)
74x2G14	dual inverter gate	schmitt trigger		6	LVC (https://assets.nexperia.com/ documents/data-sheet/74LVC2G1 4.pdf)
74x2G17	dual buffer gate	schmitt trigger		6	LVC (https://assets.nexperia.com/ documents/data-sheet/74LVC2G1 7.pdf)
74x2G32	dual 2-input OR gate			8	LVC (https://assets.nexperia.com/ documents/data-sheet/74LVC2G3 2.pdf)
74x2G34	dual buffer gate			6	LVC (https://assets.nexperia.com/ documents/data-sheet/74LVC2G3 4.pdf)
74x2G38	dual 2-input NAND gate		open- drain	8	LVC (https://assets.nexperia.com/ documents/data-sheet/74AUP2G3 8.pdf)
74x2G57	dual configurable 7-function gate	schmitt trigger		10	AUP (https://assets.nexperia.com/ documents/data-sheet/74AUP2G5 7.pdf)
74x2G58	dual configurable 7-function gate	schmitt trigger		10	AUP (https://assets.nexperia.com/ documents/data-sheet/74AUP2G5 8.pdf)
74x2G66	dual SPST analog switch	analog	analog	8	LVC (https://assets.nexperia.com/ documents/data-sheet/74LVC2G6 6.pdf)
74x2G79	dual D-type flip-flop, positive-edge trigger, Q output			8	LVC (http://www.ti.com/lit/gpn/sn74 lvc2g79)
74x2G80	dual D-type flip-flop, positive-edge trigger, Q output			8	LVC (http://www.ti.com/lit/gpn/sn74 lvc2g80)
74x2G86	dual 2-input XOR gate (a.k.a. 2-bit even-parity			8	LVC (https://assets.nexperia.com/ documents/data-sheet/74LVC2G8
	generator)				<u>6.pdf)</u>
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74x2G97	dual configurable 7-function gate	schmitt trigger		10	AUP (https://assets.nexperia.com/ documents/data-sheet/74AUP2G9 7.pdf)
74x2G98	dual configurable 7-function gate	schmitt trigger		10	AUP (https://assets.nexperia.com/ documents/data-sheet/74AUP2G9 8.pdf)
74x2G125	dual buffer, active-low enable		three- state	8	LVC (https://assets.nexperia.com/ documents/data-sheet/74LVC2G12 5.pdf)
74x2G126	dual buffer, active-high enable		three- state	8	LVC (https://assets.nexperia.com/ documents/data-sheet/74LVC2G12 6.pdf)
74x2G132	dual 2-input NAND gate	schmitt trigger		8	LVC (http://www.ti.com/lit/gpn/sn74 lvc2g132)
74x2G240	dual inverter gate, active-low enable		three- state	8	LVC (https://assets.nexperia.com/ documents/data-sheet/74LVC2G24 0.pdf)
74x2G241	dual buffer, active-low and active-high enables		three- state	8	LVC (https://assets.nexperia.com/ documents/data-sheet/74LVC2G24 1.pdf)
74x2G0604	dual combo gates - one inverter, one inverter with O.D.		open- drain	6	AUP (https://assets.nexperia.com/ documents/data-sheet/74AUP2G0 604.pdf)
74x2G3404	dual combo gates - one buffer, one inverter			6	AUP (https://assets.nexperia.com/ documents/data-sheet/74AUP2G3 404.pdf)
74x2G3407	dual combo gates - one buffer, one buffer with O.D.		open- drain	6	AUP (https://assets.nexperia.com/ documents/data-sheet/74AUP2G3 407.pdf)

Three-gate chips

All chips in this section have three gates, noted by the "3G" in the part numbers.

Part number	Description	Input	Output	Pins	Datasheet
74x3G04	triple inverter gate			8	LVC (https://assets.nexperia.com/doc uments/data-sheet/74LVC3G04.pdf)
74x3G06	triple inverter gate	schmitt trigger	open- drain	8	LVC (https://assets.nexperia.com/doc uments/data-sheet/74LVC3G06.pdf)
74x3G07	triple buffer gate	schmitt trigger	open- drain	8	LVC (https://assets.nexperia.com/doc uments/data-sheet/74LVC3G07.pdf)
74x3G14	triple inverter gate	schmitt trigger		8	LVC (https://assets.nexperia.com/doc uments/data-sheet/74LVC3G14.pdf)
74x3G16	triple buffer gate			8	LVC (https://assets.nexperia.com/doc uments/data-sheet/74LVC3G16.pdf)
74x3G17	triple buffer gate	schmitt trigger		8	LVC (https://assets.nexperia.com/doc uments/data-sheet/74LVC3G17.pdf)
74x3G34	triple buffer gate			8	LVC (https://assets.nexperia.com/doc uments/data-sheet/74LVC3G34.pdf)
74x3G0434	triple combo gates - two inverter, one buffer			8	AUP (https://assets.nexperia.com/do cuments/data-sheet/74AUP3G0434.p df)
74x3G3404	triple combo gates - two buffer, one inverter			8	AUP (https://assets.nexperia.com/do cuments/data-sheet/74AUP3G3404.p df)

Voltage translation

All chips in this section have **two** power-supply pins to translate unidirectional logic signals between two different logic voltages. The logic families that support dual-supply voltage translation are AVC, AVCH, AXC, AXCH, AXP, LVC, where the "H" in AVCH and AXCH means "bus hold" feature.

Part number	Description	Pins	AXC	АХР	LVC
74x1T45	1 buffer	6	AXC (https://w ww.ti.com/lit/gp n/SN74AXC1T 45)	AXP (https://www.nexperia.com/produc ts/analog-logic-ics/asynchronous-interf ace-logic/voltage-translators-level-shift ers/series/74AXP1T45.html)	LVC (https://w ww.ti.com/lit/gp n/SN74LVC1T4 5)
74x2T45	2 buffers	8	AXC (https://w ww.ti.com/lit/gp n/SN74AXC2T 45)	AXP (https://www.nexperia.com/produc ts/analog-logic-ics/asynchronous-interf ace-logic/voltage-translators-level-shift ers/series/74AXP2T45.html)	LVC (https://w ww.ti.com/lit/gp n/SN74LVC2T4 5)
74x4T245	4 buffers	16	AXC (https://w ww.ti.com/lit/gp n/SN74AXC4T 245)	AXP (https://www.nexperia.com/produc ts/analog-logic-ics/asynchronous-interf ace-logic/voltage-translators-level-shift ers/series/74AXP4T245.html)	n/a
74x8T245	8 buffers	24	AXC (https://w ww.ti.com/lit/gp n/SN74AXC8T 245)	AXP (https://www.nexperia.com/produc ts/analog-logic-ics/asynchronous-interf ace-logic/voltage-translators-level-shift ers/series/74AXP8T245.html)	LVC (https://w ww.ti.com/lit/gp n/SN74LVC8T2 45)
74x16T245	16 buffers	48	n/a	n/a	LVC (https://w ww.ti.com/lit/gp n/SN74LVC16T 245)

Chips in the above table support the following voltage ranges on either power supply pin:

- AXC = 0.65 to 3.6 V. Only available from Texas Instruments.
- AXP = 0.9 to 5.5 V. Only available from Nexperia.
- LVC = 1.65 to 5.5 V. Available from Diodes Inc, Nexperia, Texas Instruments.

See also

- 4000-series integrated circuits
- List of 4000-series integrated circuits
- Push-pull output, Open-collector output, Three-state output
- Schmitt trigger input
- Logic gate, Logic family
- Programmable logic device
- Pin compatibility

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