

74181, LS181, S181

Arithmetic Logic Units

4-Bit Arithmetic Logic Unit
Product Specification

Logic Products

FEATURES

- Provides 16 arithmetic operations: ADD, SUBTRACT, COMPARE, DOUBLE, plus 12 other arithmetic operations
- Provides all 16 logic operations of two variables: Exclusive-OR, Compare, AND, NAND, NOR, OR, plus 10 other logic operations
- Full lookahead carry for high-speed arithmetic operation on long words

DESCRIPTION

The '181 is a 4-bit high-speed parallel Arithmetic Logic Unit (ALU). Controlled by the four Function Select inputs ($S_0 - S_3$) and the Mode Control Input (M), it can perform all the 16 possible logic operations or 16 different arithmetic operations on active HIGH or active LOW operands. The Function Table lists these operations.

TYPE	TYPICAL PROPAGATION DELAY	TYPICAL SUPPLY CURRENT (TOTAL)
74181	22ns	91mA
74LS181	22ns	21mA
74S181	11ns	120mA

ORDERING CODE

PACKAGES	COMMERCIAL RANGE $V_{CC} = 5V \pm 5\%$; $T_A = 0^\circ C$ to $+70^\circ C$
Plastic DIP	N74181N, N74LS181N, N74S181N

NOTE:

For information regarding devices processed to Military Specifications, see the Signetics Military Products Data Manual.

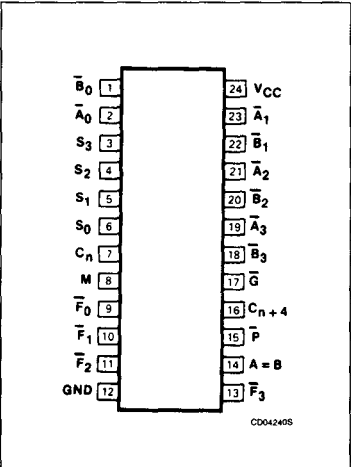
INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

PINS	DESCRIPTION	74	74S	74LS
Mode	Input	1uI	1Sul	1LSul
\bar{A} or \bar{B}	Inputs	3uI	3Sul	3LSul
S	Inputs	4uI	4Sul	4LSul
Carry	Input	5uI	5Sul	5LSul
$F_0 - F_3, = B, C_n + 4$	Outputs	10uI	10Sul	10LSul
\bar{G}	Output	10uI	10Sul	40LSul
\bar{P}	Output	10uI	10Sul	20LSul

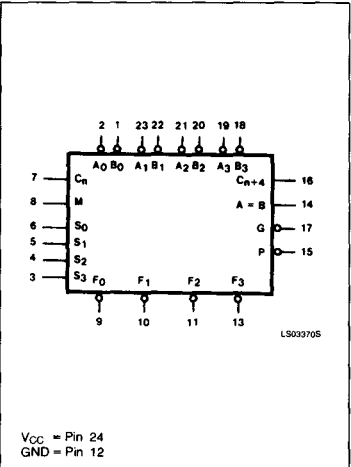
NOTE:

Where a 74 unit load (uI) is understood to be $40\mu A$ I_{IH} and $-1.6mA$ I_{IL} , a 74S unit load (Sul) is $50\mu A$ I_{IH} and $-2.0mA$ I_{IL} , and 74LS unit load (LSul) is $20\mu A$ I_{IH} and $-0.4mA$ I_{IL} .

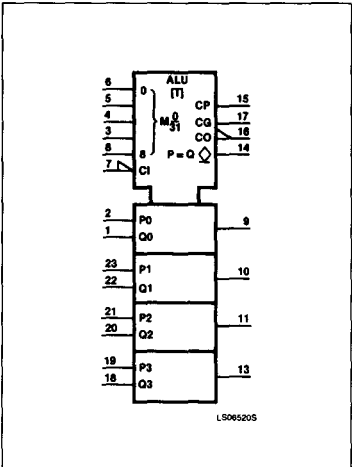
PIN CONFIGURATION



LOGIC SYMBOL



LOGIC SYMBOL (IEEE/IEC)



Arithmetic Logic Units

74181, LS181, S181

When the Mode Control input (M) is HIGH, all internal carries are inhibited and the device performs logic operations on the individual bits as listed. When the Mode Control Input is LOW, the carries are enabled and the device performs arithmetic operations on the two 4-bit words. The device incorporates full internal carry lookahead and provides for either ripple carry between devices using the $C_n + 4$ output, or for carry lookahead between packages using the signals \bar{P} (Carry Propagate) and \bar{G} (Carry Generate). \bar{P} and \bar{G} are not affected by carry in. When speed requirements are not stringent, it can be used in a simple ripple carry mode by connecting the Carry output ($C_n + 4$) signal to the Carry input (C_n) of the next unit. For high-speed operation the device is used in conjunction with the

'182 carry lookahead circuit. One carry lookahead package is required for each group of four '181 devices. Carry lookahead can be provided at various levels and offers high-speed capability over extremely long word lengths.

The $A = B$ output from the device goes HIGH when all four \bar{F} outputs are HIGH and can be used to indicate logic equivalence over 4 bits when the unit is in the subtract mode. The $A = B$ output is open collector and can be wired-AND with other $A = B$ outputs to give a comparison for more than 4 bits. The $A = B$ signal can also be used with the $C_n + 4$ signal to indicate $A > B$ and $A < B$.

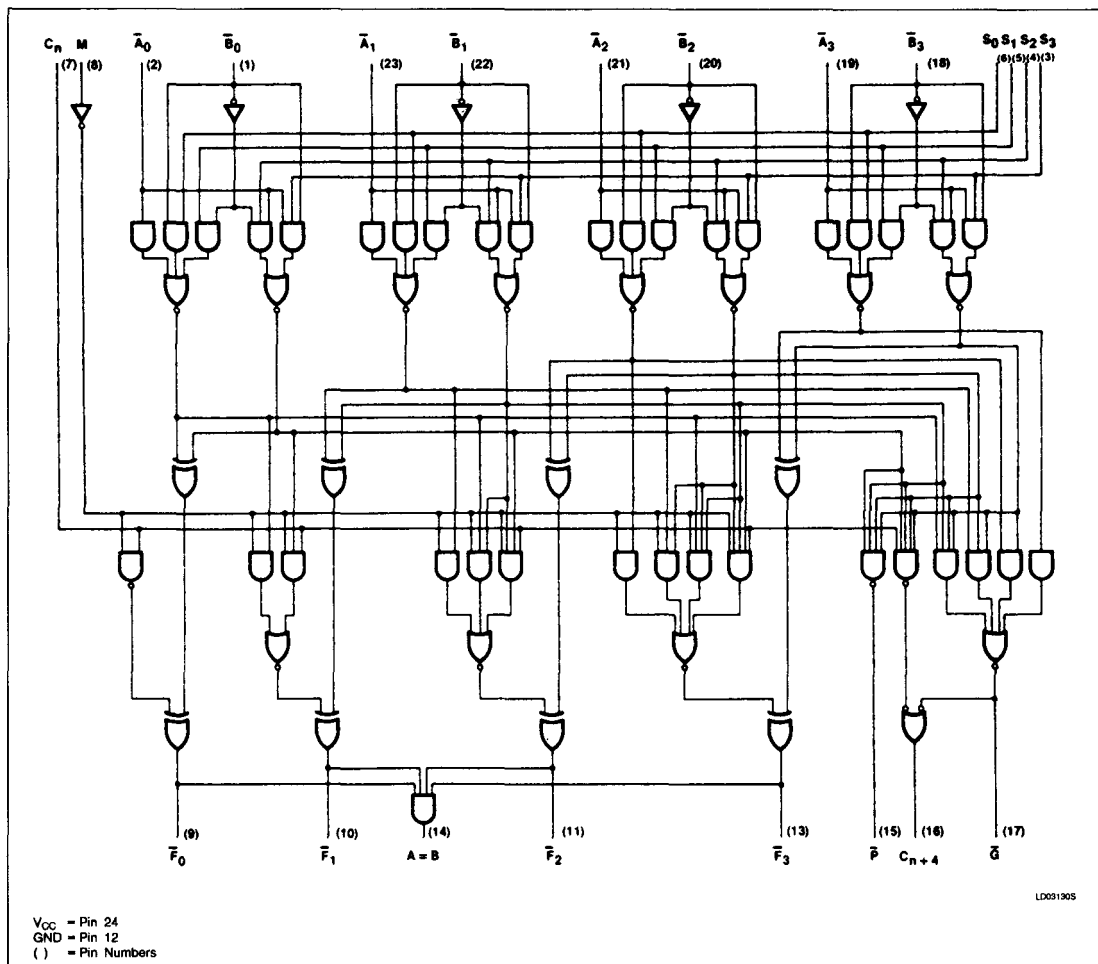
The Function Table lists the arithmetic operations that are performed without a carry in. An

incoming carry adds a one to each operation. Thus, select code LHL generates A minus B minus 1 (2s complement notation) without a carry in and generates A minus B when a carry is applied.

Because subtraction is actually performed by complementary addition (1s complement), a carry out means borrow; thus, a carry is generated when there is no underflow and no carry is generated when there is underflow.

As indicated, this device can be used with either active LOW inputs producing active LOW outputs or with active HIGH inputs producing active HIGH outputs. For either case the table lists the operations that are performed to the operands labeled inside the logic symbol.

LOGIC DIAGRAM



Arithmetic Logic Units

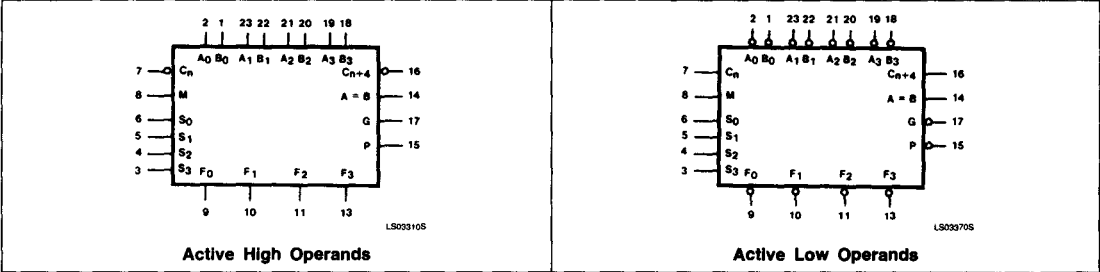
74181, LS181, S181

MODE SELECT — FUNCTION TABLE

MODE SELECT INPUTS				ACTIVE HIGH INPUTS & OUTPUTS	
S ₃	S ₂	S ₁	S ₀	Logic (M = H)	Arithmetic** (M = L) (C _n = H)
L	L	L	L	\bar{A}	A
L	L	L	H	$A + \bar{B}$	A + B
L	L	H	L	$\bar{A}B$	A + \bar{B}
L	L	H	H	Logical 0	minus 1
L	H	L	L	$\bar{A}\bar{B}$	A plus $\bar{A}\bar{B}$
L	H	L	H	\bar{B}	(A + B) plus $\bar{A}\bar{B}$
L	H	H	L	$A \odot B$	A minus B minus 1
L	H	H	H	$\bar{A}\bar{B}$	AB minus 1
H	L	L	L	$\bar{A} + B$	A plus AB
H	L	L	H	$\bar{A} \odot \bar{B}$	A plus B
H	L	H	L	B	(A + \bar{B}) plus AB
H	L	H	H	AB	AB minus 1
H	H	L	L	Logical 1	A plus A*
H	H	L	H	$A + \bar{B}$	(A + B) plus A
H	H	H	L	A + B	(A + \bar{B}) plus A
H	H	H	H	A	A minus 1

MODE SELECT INPUTS				ACTIVE LOW INPUTS & OUTPUTS	
S ₃	S ₂	S ₁	S ₀	Logic (M = H)	Arithmetic** (M = L) (C _n = L)
L	L	L	L	\bar{A}	A minus 1
L	L	L	H	$\bar{A}\bar{B}$	AB minus 1
L	L	H	L	$\bar{A} + B$	$\bar{A}\bar{B}$ minus 1
L	L	H	H	Logical 1	minus 1
L	H	L	L	$\bar{A} + \bar{B}$	A plus (A + \bar{B})
L	H	L	H	\bar{B}	AB plus (A + \bar{B})
L	H	H	L	$\bar{A} \odot \bar{B}$	A minus B minus 1
L	H	H	H	$A + \bar{B}$	A + \bar{B}
H	L	L	L	$\bar{A}\bar{B}$	A plus (A + B)
H	L	L	H	$\bar{A} \odot \bar{B}$	A plus B
H	L	H	L	B	$\bar{A}\bar{B}$ (A + B)
H	L	H	H	A + B	A + B
H	H	L	L	Logical 0	A plus A*
H	H	L	H	$\bar{A}\bar{B}$	AB plus A
H	H	H	L	AB	$\bar{A}\bar{B}$ plus A
H	H	H	H	A	A

L = LOW voltage
H = HIGH voltage level
*Each bit is shifted to the next more significant position.
**Arithmetic operations expressed in 2s complement notation.



Arithmetic Logic Units

74181, LS181, S181

ABSOLUTE MAXIMUM RATINGS (Over operating free-air temperature range unless otherwise noted.)

PARAMETER		74	74LS	74S	UNIT
V _{CC}	Supply voltage	7.0	7.0	7.0	V
V _{IN}	Input voltage	-0.5 to +5.5	-0.5 to +5.5	-0.5 to +5.5	V
I _{IN}	Input current	-30 to +5	-30 to +1	-30 to +5	mA
V _{OUT}	Voltage applied to output in HIGH output state	-0.5 to +V _{CC}	-0.5 to +V _{CC}	-0.5 to +V _{CC}	V
T _A	Operating free-air temperature range	0 to 70			°C

RECOMMENDED OPERATING CONDITIONS

PARAMETER		74			74LS			74S			UNIT
		Min	Nom	Max	Min	Nom	Max	Min	Nom	Max	
V _{CC}	Supply voltage	4.75	5.0	5.25	4.75	5.0	5.25	4.75	5.0	5.25	V
V _{IH}	HIGH-level input voltage	2.0			2.0			2.0			V
V _{IL}	LOW-level input voltage			+0.8			+0.8			+0.8	V
I _{IK}	Input clamp current			-12			-18			-18	mA
I _{OH}	HIGH-level output current			-800			-400			-1000	μA
I _{OL}	LOW-level output current			16			8			20	mA
T _A	Operating free-air temperature	0		70	0		70	0		70	°C

SUM MODE TEST TABLE I**FUNCTION INPUTS:** S₀ = S₃ = 4.5V, S₁ = S₂ = M = 0V

PARAMETER	INPUT UNDER TEST	OTHER INPUT, SAME BIT		OTHER DATA INPUTS		OUTPUT UNDER TEST
		Apply 4.5V	Apply GND	Apply 4.5V	Apply GND	
t _{PLH} t _{PHL}	\bar{A}_i	\bar{B}_i	None	Remaining \bar{A} and \bar{B}	C _n	\bar{F}_i
t _{PLH} t _{PHL}	\bar{B}_i	\bar{A}_i	None	Remaining \bar{A} and \bar{B}	C _n	\bar{F}_i
t _{PLH} t _{PHL}	\bar{A}_i	\bar{B}_i	None	None	Remaining \bar{A} and \bar{B} , C _n	\bar{P}
t _{PLH} t _{PHL}	\bar{B}_i	\bar{A}_i	None	None	Remaining \bar{A} and \bar{B} , C _n	\bar{P}
t _{PLH} t _{PHL}	\bar{A}_i	None	\bar{B}_i	Remaining \bar{B}	Remaining \bar{A} , C _n	\bar{G}
t _{PLH} t _{PHL}	\bar{B}_i	None	\bar{A}_i	Remaining \bar{B}	Remaining \bar{A} , C _n	\bar{G}
t _{PLH} t _{PHL}	\bar{A}_i	None	\bar{B}_i	Remaining \bar{B}	Remaining \bar{A} , C _n	C _n + 4
t _{PLH} t _{PHL}	\bar{B}_i	None	\bar{A}_i	Remaining \bar{B}	Remaining \bar{A} , C _n	C _n + 4
t _{PLH} t _{PHL}	C _n	None	None	All \bar{A}	All \bar{B}	Any \bar{F} or C _n + 4

Arithmetic Logic Units

74181, LS181, S181

DIFF MODE TEST TABLE II

FUNCTION INPUTS: $S_0 = S_3 = 4.5V$, $S_1 = S_2 = M = 0V$

PARAMETER	INPUT UNDER TEST	OTHER INPUT, SAME BIT		OTHER DATA INPUTS		OUTPUT UNDER TEST
		Apply 4.5V	Apply GND	Apply 4.5V	Apply GND	
t_{PLH} t_{PHL}	\bar{A}_i	None	\bar{B}_i	Remaining \bar{A}	Remaining \bar{B} , C_n	\bar{F}_i
t_{PLH} t_{PHL}	\bar{B}_i	\bar{A}_i	None	Remaining \bar{A}	Remaining \bar{B} , C_n	\bar{F}_i
t_{PLH} t_{PHL}	\bar{A}_i	None	\bar{B}_i	None	Remaining \bar{A} and \bar{B} , C_n	\bar{P}
t_{PLH} t_{PHL}	\bar{B}_i	\bar{A}_i	None	None	Remaining \bar{A} and \bar{B} , C_n	\bar{P}
t_{PLH} t_{PHL}	\bar{A}_i	\bar{B}_i	None	None	Remaining \bar{A} and \bar{B} , C_n	\bar{G}
t_{PLH} t_{PHL}	\bar{B}_i	None	\bar{A}_i	None	Remaining \bar{A} and \bar{B} , C_n	\bar{G}
t_{PLH} t_{PHL}	\bar{A}_i	None	\bar{B}_i	Remaining \bar{A}	Remaining \bar{B} , C_n	$A = B$
t_{PLH} t_{PHL}	\bar{B}_i	\bar{A}_i	None	Remaining \bar{A}	Remaining \bar{B} , C_n	$A = B$
t_{PLH} t_{PHL}	\bar{A}_i	\bar{B}_i	None	None	Remaining \bar{A} and \bar{B} , C_n	$C_n + 4$
t_{PLH} t_{PHL}	\bar{B}_i	None	\bar{A}_i	None	Remaining \bar{A} and \bar{B} , C_n	$C_n + 4$
t_{PLH} t_{PHL}	C_n	None	None	All \bar{A} and \bar{B}	None	Any \bar{F} or $C_n + 4$

LOGIC MODE TEST TABLE III

PARAMETER	INPUT UNDER TEST	OTHER INPUT, SAME BIT		OTHER DATA INPUTS		OUTPUT UNDER TEST	FUNCTION INPUTS
		Apply 4.5V	Apply GND	Apply 4.5V	Apply GND		
t_{PLH} t_{PHL}	\bar{A}_i	\bar{B}_i	None	None	Remaining \bar{A} and \bar{B} , C_n	\bar{F}_i	$S_1 = S_2 = M = 4.5V$ $S_0 = S_3 = 0V$
t_{PLH} t_{PHL}	\bar{B}_i	\bar{A}_i	None	None	Remaining \bar{A} and \bar{B} , C_n	\bar{F}_i	$S_1 = S_2 = M = 4.5V$ $S_0 = S_3 = 0V$

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74181, LS181, S181

DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

PARAMETER	TEST CONDITIONS ¹		74181			74LS181			74S181			UNIT
			Min	Typ ²	Max	Min	Typ ²	Max	Min	Typ ²	Max	
V_{OH} HIGH-level output voltage	$V_{CC} = \text{MIN}$, $V_{IH} = \text{MIN}$, $V_{IL} = \text{MAX}$, $I_{OH} = \text{MAX}$	Any output except A = B	2.4	3.4		2.7	3.4		2.7	3.4		V
V_{OL} LOW-level output voltage	$V_{CC} = \text{MIN}$, $V_{IH} = \text{MIN}$, $V_{IL} = \text{MAX}$	$I_{OL} = \text{MAX}$ All outputs		0.2	0.4		0.35	0.5			0.5	V
		$I_{OL} = 4\text{mA}$					0.25	0.4				V
		$I_{OL} = 16\text{mA}$ G output					0.47	0.7				V
		$I_{OL} = 8\text{mA}$ P output					0.35	0.5				V
V_{IK} Input clamp voltage	$V_{CC} = \text{MIN}$, $I_I = I_{IK}$				-1.5			-1.5			-1.2	V
I_I Input current at maximum input voltage	$V_{CC} = \text{MAX}$	Mode input			1.0			0.1			1.0	mA
		\bar{A} or \bar{B} inputs			1.0			0.3			1.0	mA
		S inputs			1.0			0.4			1.0	mA
		Carry input			1.0			0.5			1.0	mA
I_{IH} HIGH-level input current	$V_{CC} = \text{MAX}$	$V_I = 2.4\text{V}$			40							μA
					120							μA
					160							μA
					200							μA
		$V_I = 2.7\text{V}$						20			50	μA
								60			150	μA
								80			200	μA
								100			250	μA
I_{IL} LOW-level input current	$V_{CC} = \text{MAX}$	$V_I = 0.4\text{V}$			-1.6			-0.4				mA
					-4.8			-1.2				mA
					-6.4			-1.6				mA
					-8			-2				mA
		$V_I = 0.5\text{V}$									-2	mA
											-6	mA
											-8	mA
											-10	mA
I_{OH} HIGH-level output current	$V_{IH} = \text{MIN}$, $V_{IL} = \text{MAX}$, $V_{OH} = 5.5\text{V}$ A = B only				250			100			250	μA
I_{OS} Short-circuit output current ³	$V_{CC} = \text{MAX}$ Any output except A = B		-18		-57	-15		-100	-40		-100	mA
I_{CC} Supply current ⁴ (total)	$V_{CC} = \text{MAX}$	Note 4a		88	140		20	34		120	220	mA
		Note 4b		94	150		21	37		120	220	mA

NOTES:

- For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
- All typical values are at $V_{CC} = 5\text{V}$, $T_A = 25^\circ\text{C}$.
- I_{OS} is tested with $V_{OUT} = +0.5\text{V}$ and $V_{CC} = V_{CC\text{ MAX}} + 0.5\text{V}$. Not more than one output should be shorted at a time and duration of the short circuit should not exceed one second.
- I_{CC} is measured with the following conditions: a. S_0 through S_3 , M, and A inputs are at 4.5V, other inputs grounded, all outputs open. b. S_0 through S_3 and M inputs are at 4.5V, other inputs grounded, all outputs open.

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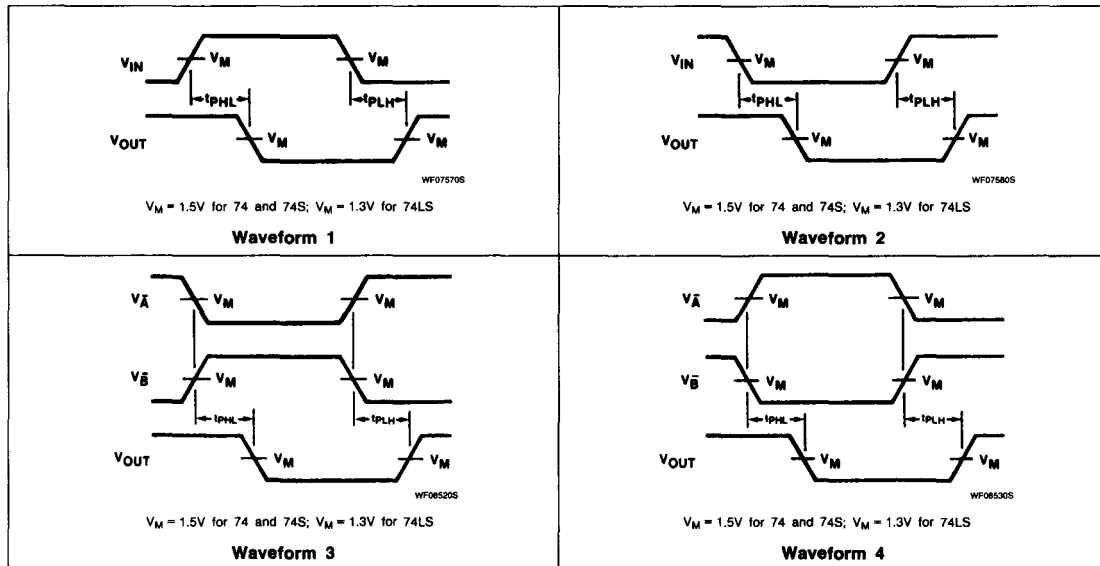
AC ELECTRICAL CHARACTERISTICS $T_A = 25^\circ\text{C}$, $V_{CC} = 5.0\text{V}$

PARAMETER		TEST CONDITIONS	74		74LS		74S		UNIT
			$C_L = 15\text{pF}$ $R_L = 400\Omega$		$C_L = 15\text{pF}$ $R_L = 2\text{k}\Omega$		$C_L = 15\text{pF}$ $R_L = 280\Omega$		
			Min	Max	Min	Max	Min	Max	
t_{PLH} t_{PHL}	Propagation delay C_n to C_{n+4}	M = 0V, Sum or Diff Mode see Waveform 2 and Tables I & II		18 19		27 20		10.5 10.5	ns
t_{PLH} t_{PHL}	Propagation delay C_n to F outputs	M = 0V, Sum or Diff Mode see Waveform 2 and Tables I & II		19 18		26 20		12 12	ns
t_{PLH} t_{PHL}	Propagation delay \bar{A} or \bar{B} inputs to \bar{G} output	M = $S_1 = S_2 = 0\text{V}$, $S_0 = S_3 = 4.5\text{V}$ Sum Mode, see Waveform 2 and Table I		19 19		29 23		12 12	ns
t_{PLH} t_{PHL}	Propagation delay \bar{A} or \bar{B} inputs to \bar{G} output	M = $S_0 = S_3 = 0\text{V}$, $S_1 = S_2 = 4.5\text{V}$ Diff Mode, see Waveform 3 and Table II		25 25		32 32		15 15	ns
t_{PLH} t_{PHL}	Propagation delay \bar{A} or \bar{B} inputs to \bar{P} output	M = $S_1 = S_2 = 0\text{V}$, $S_0 = S_3 = 4.5\text{V}$ Sum Mode, see Waveform 2 and Table I		19 25		30 30		12 12	ns
t_{PLH} t_{PHL}	Propagation delay \bar{A} or \bar{B} inputs to \bar{P} output	M = $S_0 = S_3 = 0\text{V}$, $S_1 = S_2 = 4.5\text{V}$ Diff Mode, see Waveform 3 and Table II		25 25		30 33		15 15	ns
t_{PLH} t_{PHL}	Propagation delay \bar{A}_i or \bar{B}_i inputs to \bar{F}_i outputs	M = $S_1 = S_2 = 0\text{V}$, $S_0 = S_3 = 4.5\text{V}$ Sum Mode, see Waveform 2 and Table I		42 32		32 20		16.5 16.5	ns
t_{PLH} t_{PHL}	Propagation delay \bar{A}_i or \bar{B}_i inputs to \bar{F}_i outputs	M = $S_0 = S_3 = 0\text{V}$, $S_1 = S_2 = 4.5\text{V}$ Diff Mode, see Waveform 3 and Table II		48 34		32 32		20 22	ns
t_{PLH} t_{PHL}	Propagation delay \bar{A}_i or \bar{B}_i inputs to \bar{F}_i outputs	M = 4.5V, Logic Mode see Waveform 2 and Table III		48 34		33 38		20 22	ns
t_{PLH} t_{PHL}	Propagation delay \bar{A} or \bar{B} inputs to C_{n+4} output	M = 0V, $S_0 = S_3 = 4.5\text{V}$, $S_1 = S_2 = 0\text{V}$ Sum Mode, see Waveform 1 and Table I		43 41		38 38		18.5 18.5	ns
t_{PLH} t_{PHL}	Propagation delay \bar{A} or \bar{B} inputs to C_{n+4} outputs	M = 0V, $S_0 = S_3 = 0\text{V}$, $S_1 = S_2 = 4.5\text{V}$ Diff Mode, see Waveform 4 and Table II		50 50		41 41		23 23	ns
t_{PLH} t_{PHL}	Propagation delay \bar{A} or \bar{B} inputs to A = B output	M = $S_0 = S_3 = 0\text{V}$, $S_1 = S_2 = 4.5\text{V}$ Diff Mode, see Waveform 3 and Table II		50 48		50 62		23 30	ns

Arithmetic Logic Units

74181, LS181, S181

AC WAVEFORMS



TEST CIRCUITS AND WAVEFORMS

